



<Variant Name>



Title :

RF BD

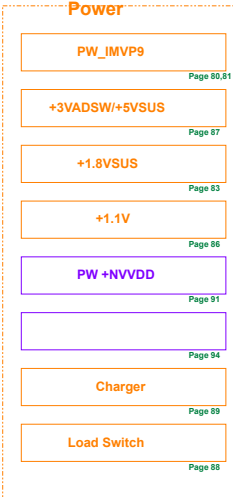
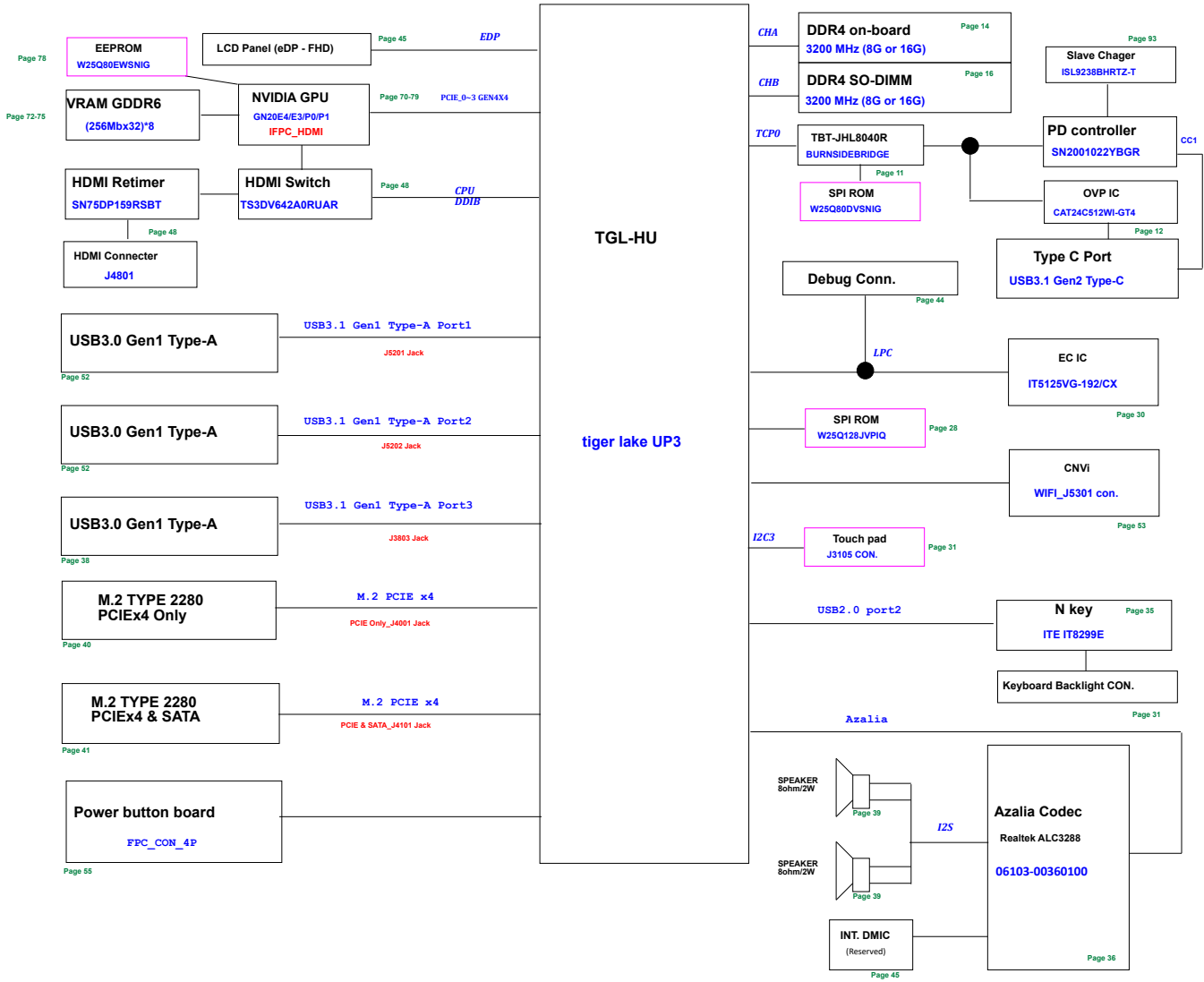
NB1-RD3EE2

Engineer: EE

Size	Project Name	Rev
A	UX482	R0.1

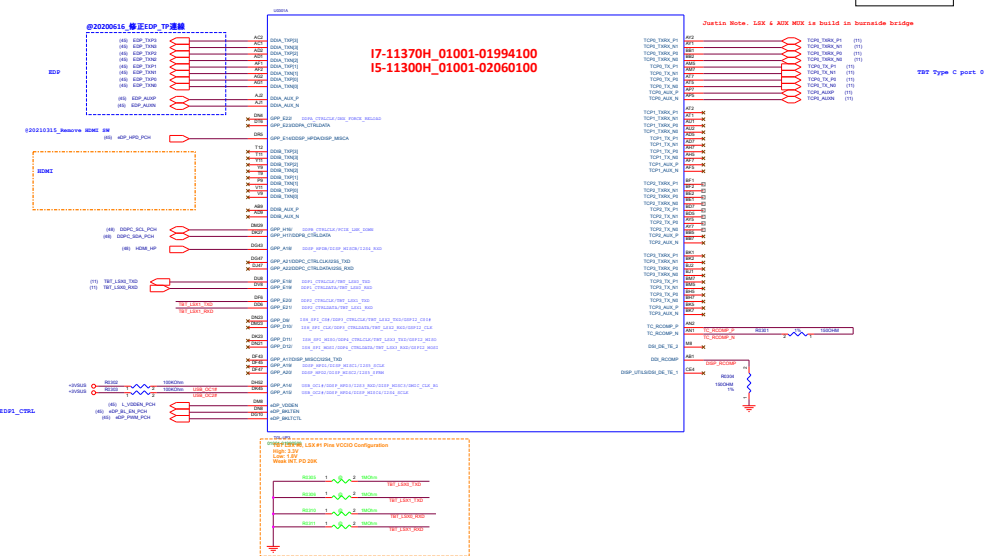
FX516 SCHEMATIC

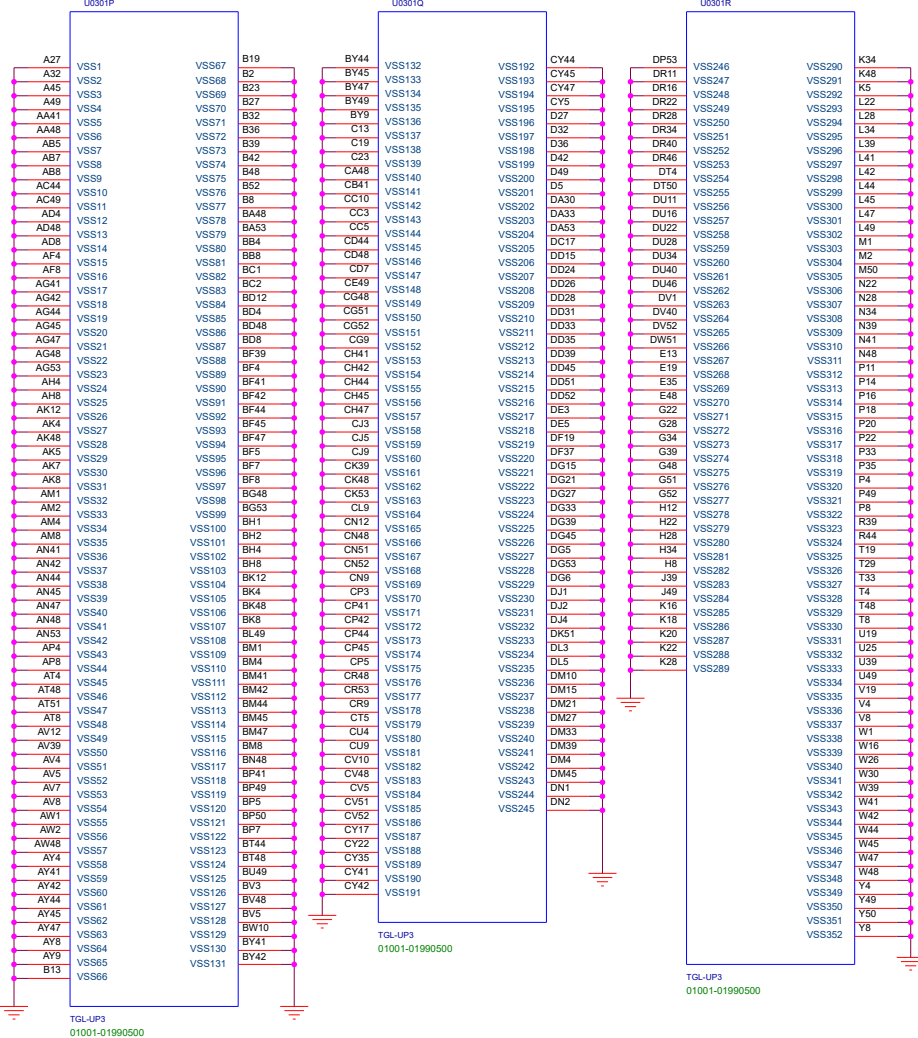
BLOCK DIAGRAM



- 80_PW_IMVP8 (1)
- 81_PW_IMVP8 (2)
- 83_PW_+1.0VSUS / +1.8VSUS
- 86_PW_1.2V/+0.6VS
- 87_PW_+3VADSW/+5VSUS
- 88_PW_LOAD SWITCH
- 89_PW_CHARGER(BQ24780)
- 90_PW_PROTECTION

- 91_PW_NVVDD
- 94_PW_VRAM

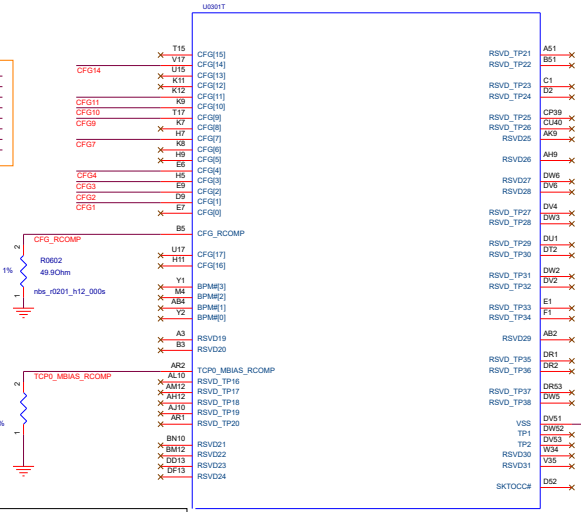
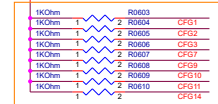




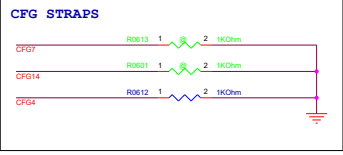
<Variant Name>

ASUS		Project Name	Rev
UX482			R0.1
Title : CPU_PCH_POEWR,GND			
Size	Dept.:	Engineer:	EE
C	NB1-RD3EE2		
Date: Wednesday, March 17, 2021	Sheet	5	of 102

VCCIO_OUT



#20200629 公版並未接地, follo UX482 但預留0 ohm



TGL-UP3 01001-01990500			
	1	0	NOTE
CFG4	DISABLE	ENABLE	eDP ENABLE

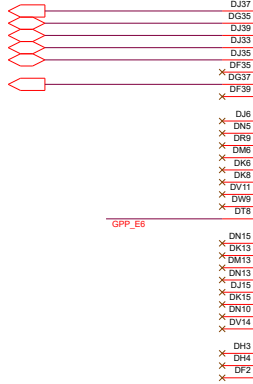
CFG	Description	Termination	Resistor
	Operation; No stall. - 0 = Stall		
CFG[0]	RSVD	None	
CFG[1]	RSVD	Pull-up to VCCIO	1K ohm
CFG[2]	RSVD	Pull-up to VCCIO	1K ohm
CFG[3]	RSVD	Pull-up to VCCIO	1K ohm
CFG[4]	eDP enable Strap: - 1 = Disabled. - 0 = Enabled.	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[6:5]	RSVD	None	
CFG[7]	PEG deferred link training	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[8]	RSVD	None	
CFG[11:9]	RSVD	Pull-up to VCCIO	1K ohm
CFG[13:12]	RSVD	None	
CFG[14]	PEG60 Lane Reversal: - 1 - (Default) Normal - 0 - Reversed	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[1 7:15]	RSVD	None	

CFG[7] Training:
- 1 = (default) PEG Train Impairment
- 0 = PEG Wait for BIOS for Training

<Variant Name>

To ROM/TPM

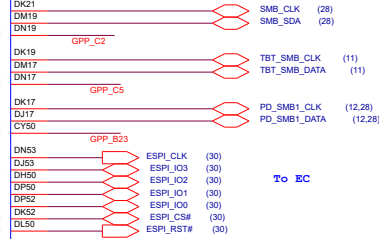
(28) SPI_CLK_SPI
(28) PCH_SPI_DQ3
(28) PCH_SPI_DQ2
(28) SPI_SO_SPI
(28) SPI_SI_SPI
(28) SPI_CS#0_SPI



TGLUP3
01001-01990500

GPP_B23/SM1ALERT#/PCHHOT#
GPP_A2/ESP1_I02/SUBNARH#

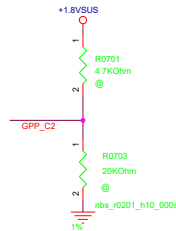
GPP_C0/SMBCLK
GPP_C1/SMBDATA
GPP_C2/SMBALERT#
GPP_C3/SMLDCLK
GPP_C4/SMLD0DATA
GPP_C5/SMLD1ALERT#
GPP_C6/SML1CLK
GPP_C7/SML1DATA
/GSPH1_CS1#
GPP_A5/ESPI_CLK
GPP_A3/ESPI_I03/SUSACK#
GPP_A1/ESPI_I01
GPP_A0/ESPI_I00
GPP_A5/ESPI_CS#
GPP_A6/ESPI_RESET#



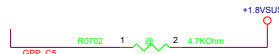
To EC

VPRO ENABLE STRAP

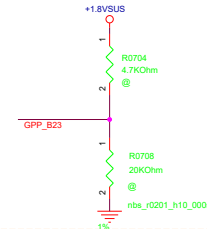
TLS CONFIDENTIALITY
LOW: TLS CONFIDENTIALITY DISABLE
HIGH: TLS CONFIDENTIALITY ENABLE
WEAK INT.PD 20K
Must be pulled up to support
Intel AMT with TLS.



BFX STRAP 1 -BIT1 WEAK INT.PD 20K



CFUNSSC CLOCK FREQ
HIGH:19.2MHZ CLOCK FROM DIVIDER
(DERIVED FROM 38.4MHZ CRYSTAL)
LOW: 38.4MHZ CLOCK FROM DIRECT CRYSTAL (DEFAULT)
WEAK INT.PD 20K

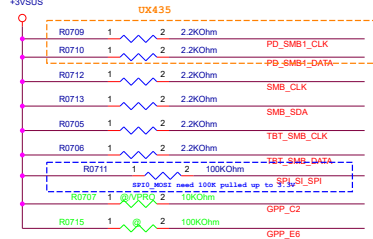


To SO-DIMM

Reserved for TBT Vpro

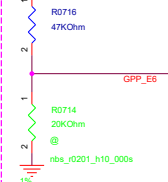
to PD

+3VSUS



+1.8VSUS

Follow Intel TGL-UP3 CRB



<Variant Name>

Project Name		Rev
ASUS UX482		R0.1

Title :		CPU LPC,SPI,SMB,CLINK
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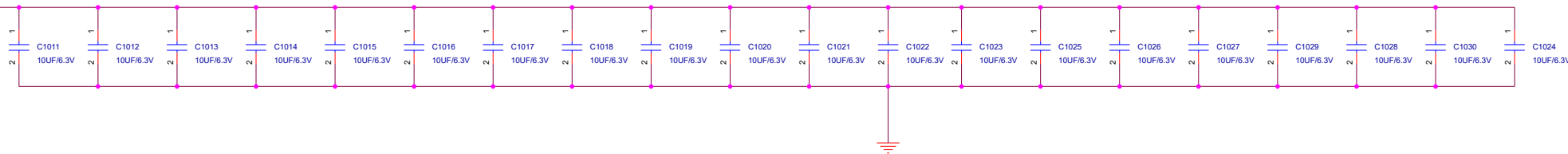
Size	Dept.:	Engineer:
C	NB1-RD3EE2	EE

Date: Wednesday, March 17, 2021	Sheet	7	of	102
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+VCCIN

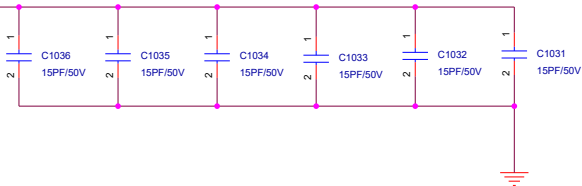
TGL UP3 ICmax=65A (0402 10uF *12)



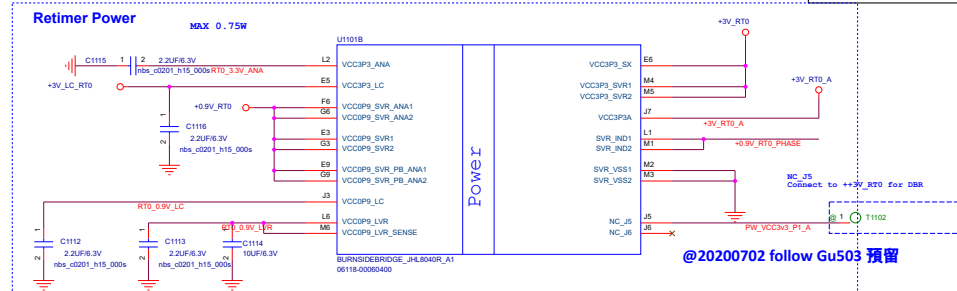
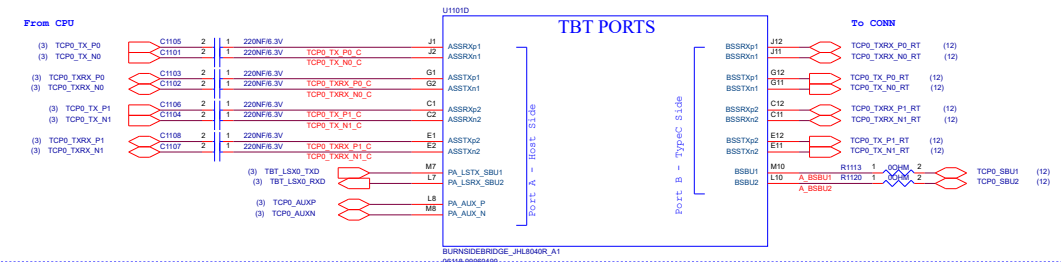
@20200616_add C1031~36: 15PF for EMI/RF

+VCCIN

TGL IVR decoupling Caps



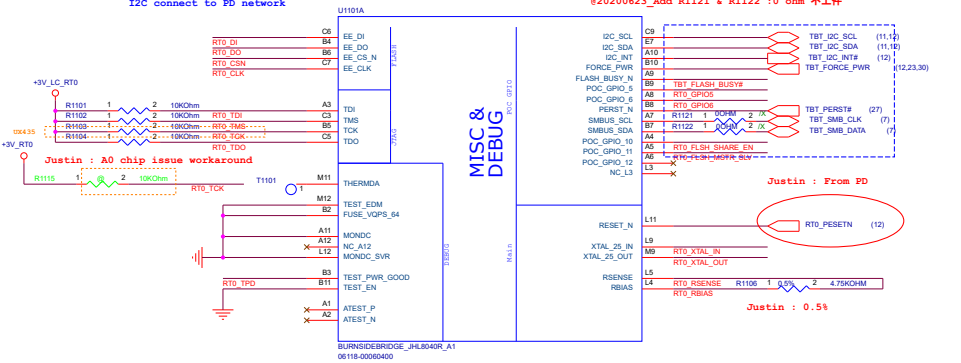
20GBPS TBT LINK PORT 0



MISC Justin: SMBUS for Vpro

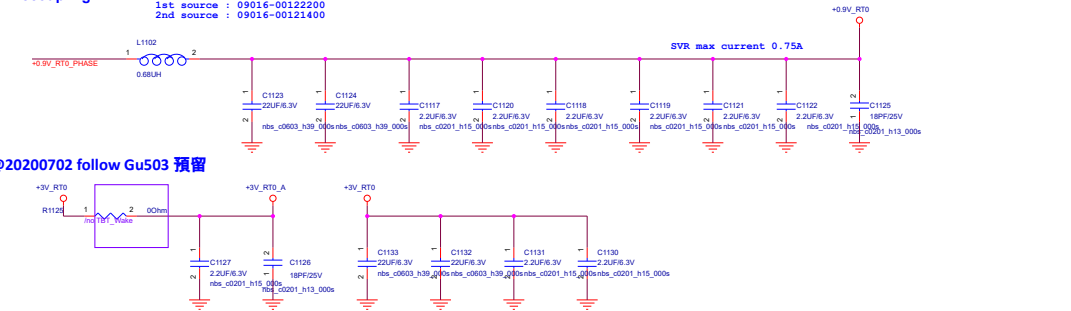
Justin: SMBUS for Vpro

I2C connect to PD network



Decoupling

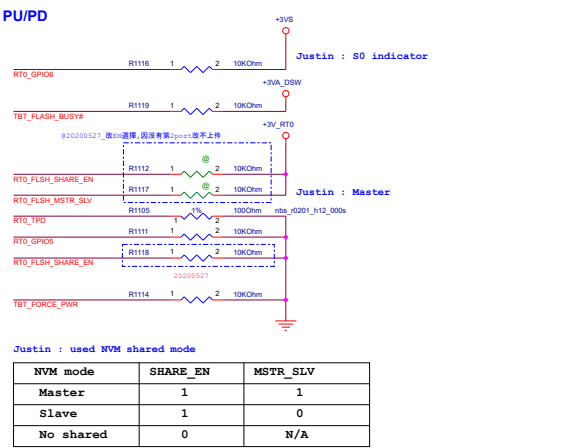
```
[Inductor colay footprint] R1.0E
1st source : 09016-00122200
2nd source : 09016-00121400
```



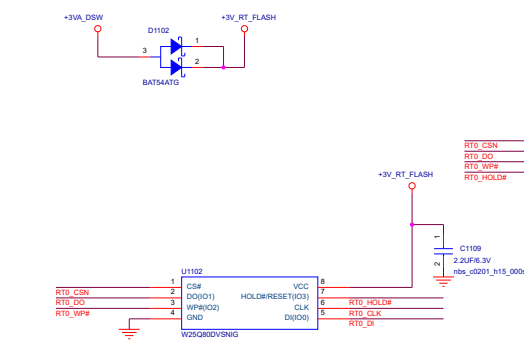
@20200702 follow Gu503 預留

@20200611_C1110 & C1111 將18PF改22PCF

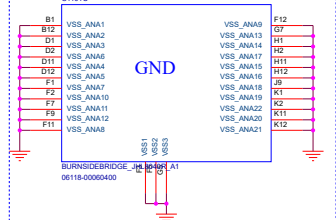
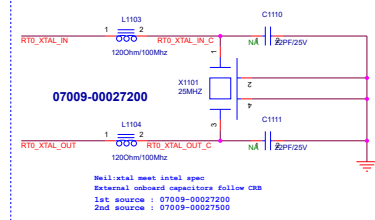
PU/PD



Flash ROM

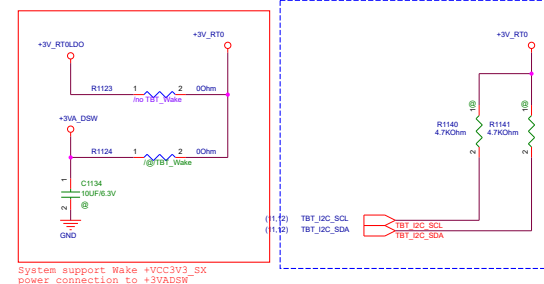


25Mhz Xtal



@2020831_TBT_I2C_SCL/TBT_I2C_SDA PU +3V_RT0

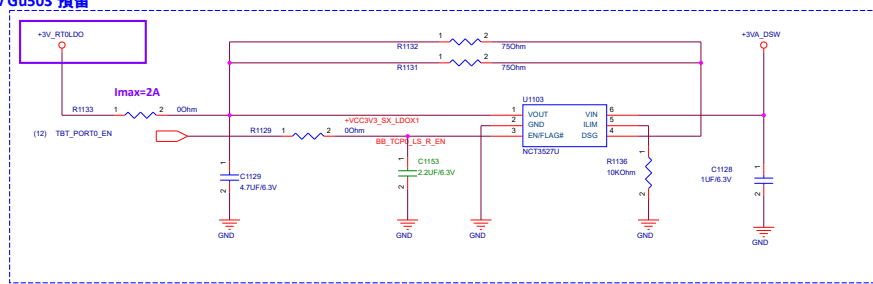
@20200702 follow Gu503 預留

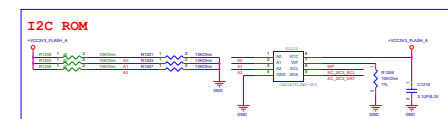
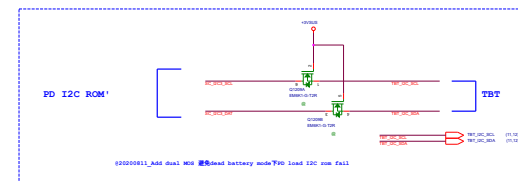
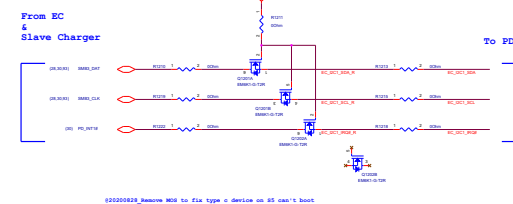
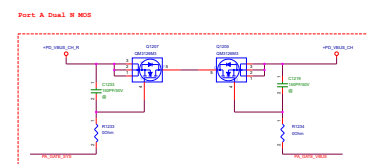
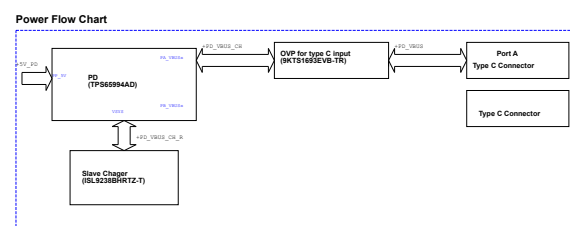
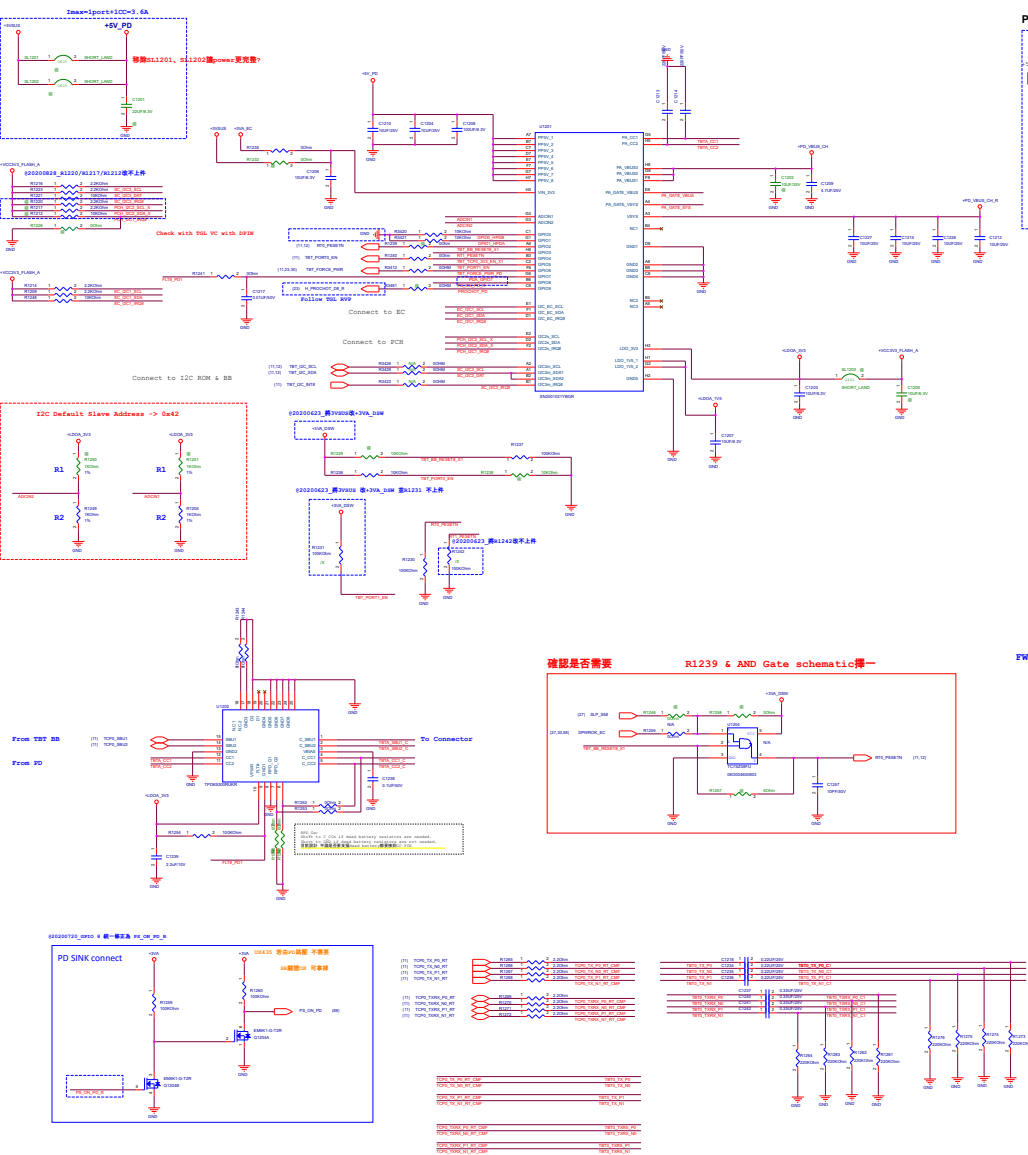


System support Wake +VCC3V3_SX
power connection to +3VADSW

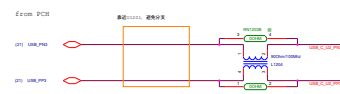
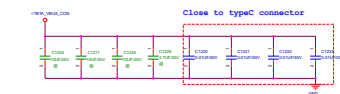
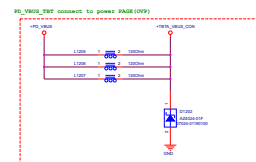
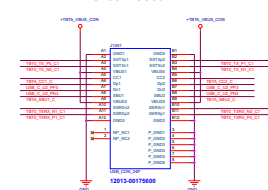
@20200702 follow Gu503 預留


Check which power solution should be used





TYPE-C Connector



		Title : DDR4_TERMINATION	
ASUSTeK COMPUTER INC.		Engineer: EE	
Size A	Project Name GX502GX		Rev R1.2
Date: Wednesday, March 17, 2021		Sheet 13 of 102	

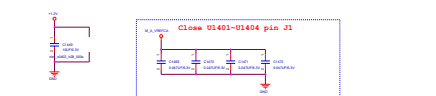
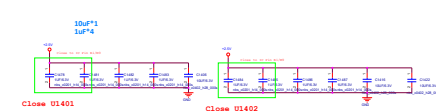
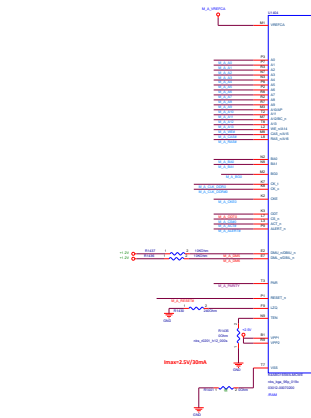
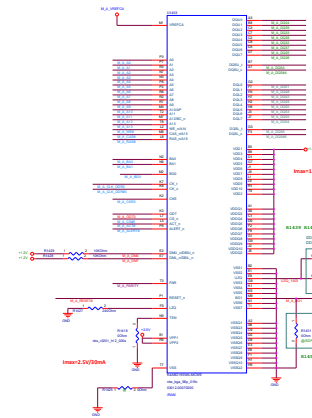
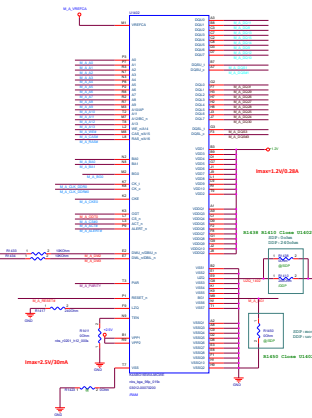
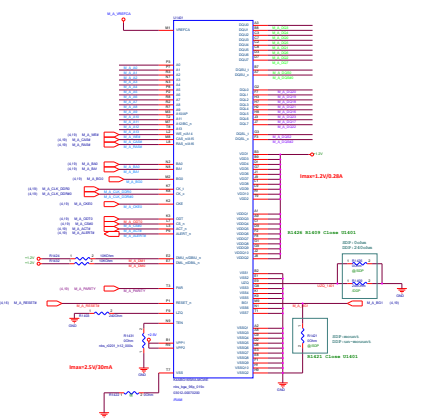
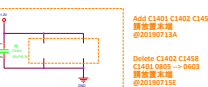


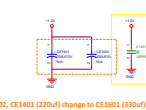
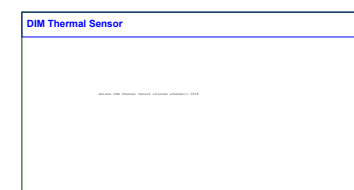
Table 4-25. DDR4 Memory Down Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x pF (min)	Note
DDR4 Memory Down (4B 2 Banks) per Channel	VDDQ/VDD	4 as near each all DIMM device as possible	66x 1uF (0402) (min of 48 uFuff)	
	VDDQ/VDD	Distributed around the DIMM device	20x 10uF (0603) (min of 12 uFuff)	
	VPP	2 as near each all DIMM device as possible	32x 1uF (0402)	
	VPP	Distributed around the DIMM device	10x 10uF (0603)	
VT	VT	Distributed along termination resistors	32x 1uF (0402)	
	VT	Distributed evenly across domain	8x 10uF (0603)	



Add C1401 C1402 C1458
删除电容
@20190713A


Delete C1402 C1458
删除电容
@20190713E




CE1402, CE1401 (220uF) change to CE1601 (330uF)
@20190626A



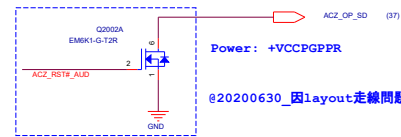
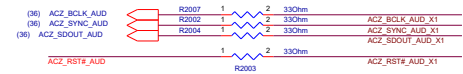
<Variant Name>

		Title : DDR4_ON-BOARD_A2	
NB1-RD3EE2		Engineer: EE	
Size Custom	Project Name UX482		Rev R0.1
Date: Wednesday, March 17, 2021		Sheet 15 of 102	

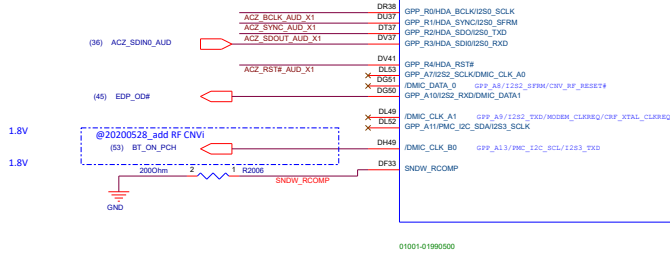
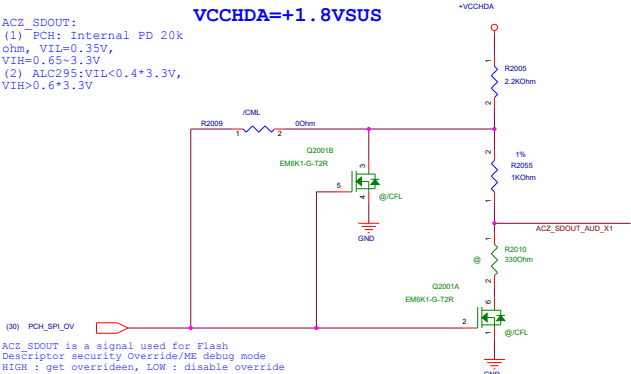
<Variant Name>

		Title : DDR4_ON-BOARD_A2	
NB1-RD3EE2		Engineer: EE	
Size Custom	Project Name UX482		Rev R0.1
Date: Wednesday, March 17, 2021		Sheet 17 of 102	

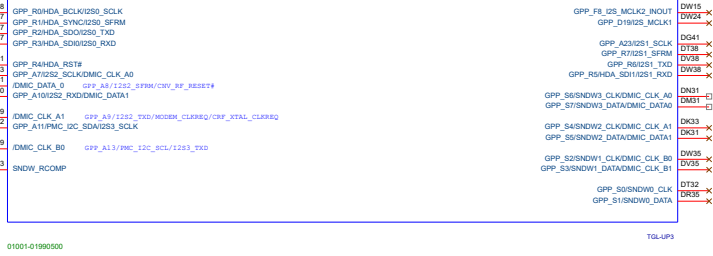
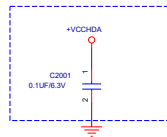
HD Audio



@20200817_Follow Gaming畫法



@20200612_add C2001 for CRB
close to the PCH ball



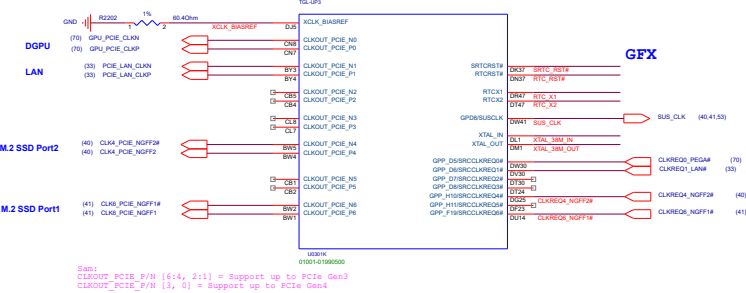
<Variant Name>

Project Name		Rev
ASUS		UX482
Title :		CPU_PCH_AUDIO.S010.S0XC
Size	Dept.:	Engineer:
D	NB1-RD3EE2	EE
Date: Wednesday, March 17, 2021	Sheet	20 of 102



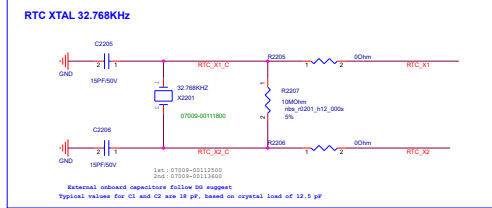
USB 2.0		USB 3.0	
1	IO Type A	USB3_1	USB 3.1 Port (IO)
2	TypeC port0	USB3_2	
4	TypeC port1	USB3_3	
5	Camera	USB3_4	
6	Card Reader		
7			
8			
9			
10			

TCSS (CPU)	
TCPS	MB TypeC port0
TCPI	MB TypeC port1
TCPI	
TCPS	

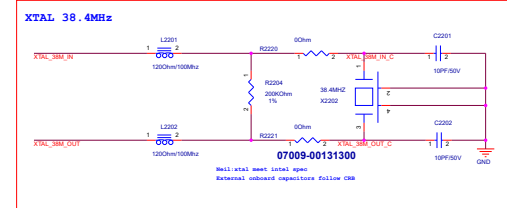


• CLKOUT_PCIE_P/N [3, 0] = Must be used for PCIe* Gen4 support
 Any un-used CLKOUT_PCIE_P/N differential pair not being routed on a platform should be configured as "Disabled" through the Intel® Flash Image Tool (FIT) tool. The CLKOUT_PCIE_P/N differential pairs are called out as CLKOUT_SRC differential outputs in FIT as discussed in the SPI Programming Guide.

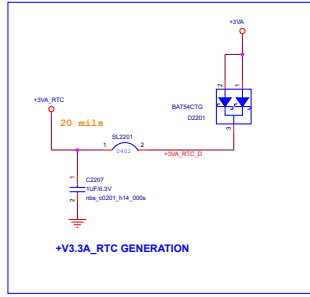
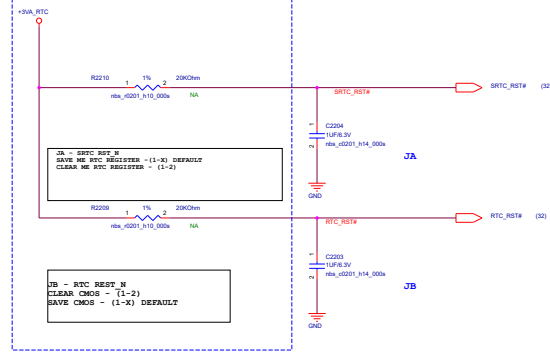
@20200630_XTAL change 07009-0011800 & 15PF for UX482



@20200630_C22016 C2202 Change 10PF for UX482 R1.1

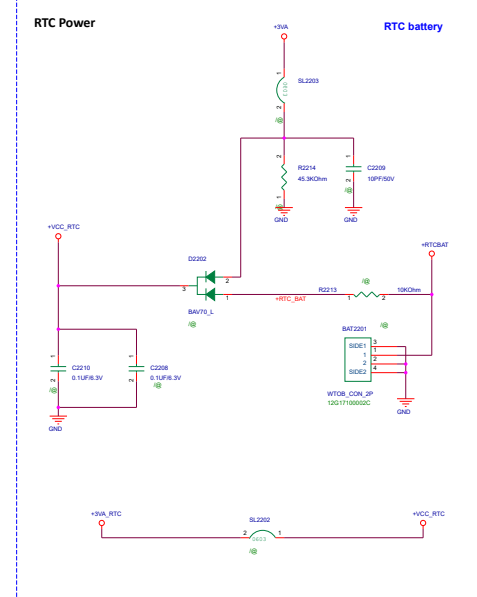


@20200611_R2209 & R2210 27K 20K for CMB

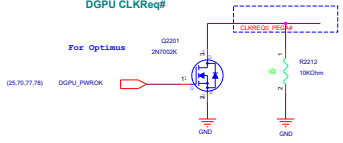


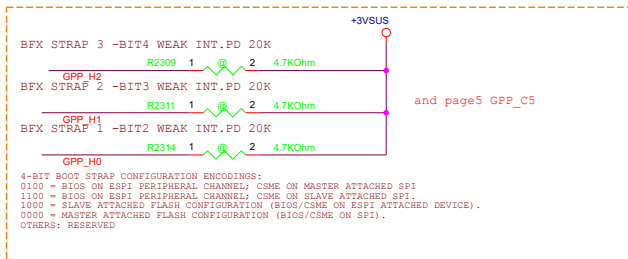
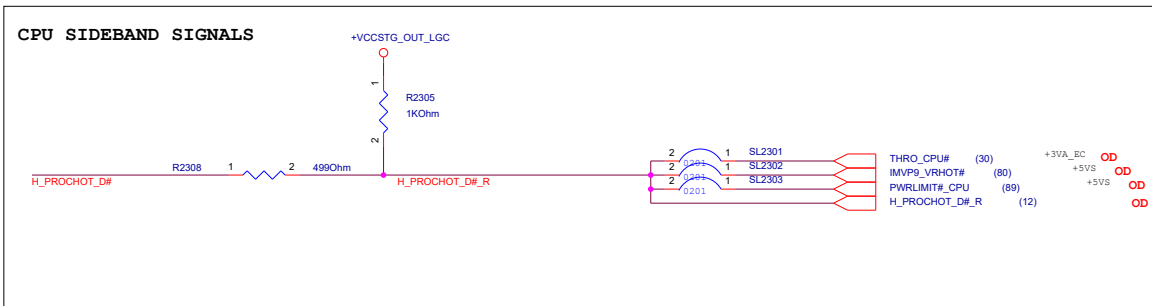
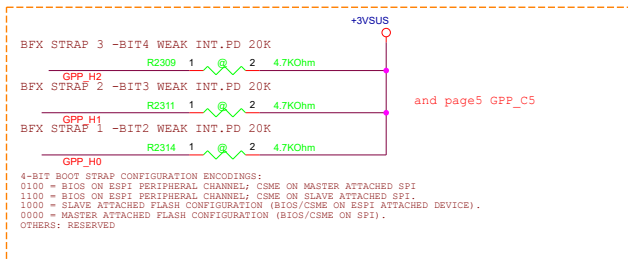
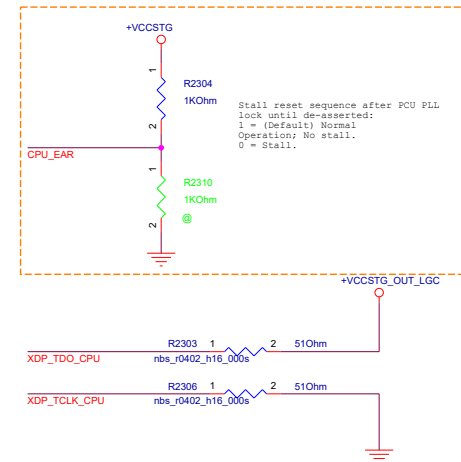
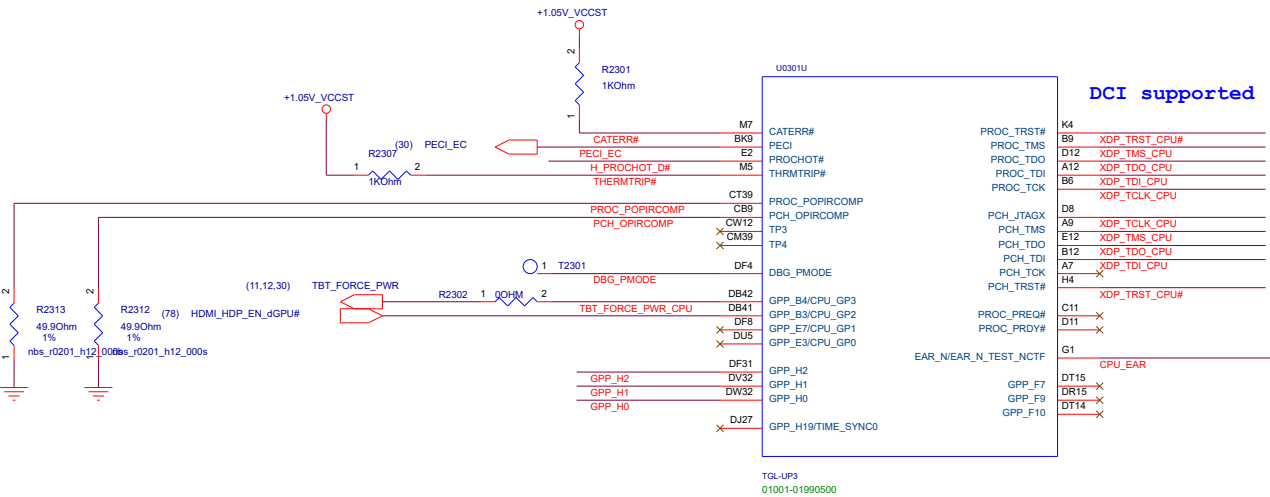
Justin : No used divided resistors. PCH has Rload inside and +3VA PU will cause VCCRTC drop to 2.7V in S0
 VCCRTC must not exceed 3.3V and sustained operation at voltages below 3.0V is not recommended
 Intel suggested to use diode circuit for long life reliability

@20200702_add RTC battery



@20200630_change name CLKREQ0_PEGA#





<Variant Name>

<Variant Name>



Project Name

UX482

Rev

R0.1

Title : **PCH-SPI ROM,OTH**

Size

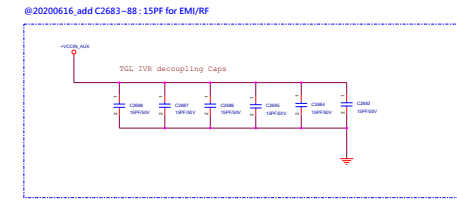
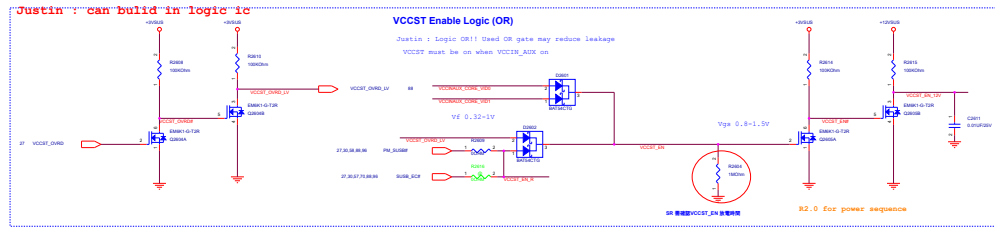
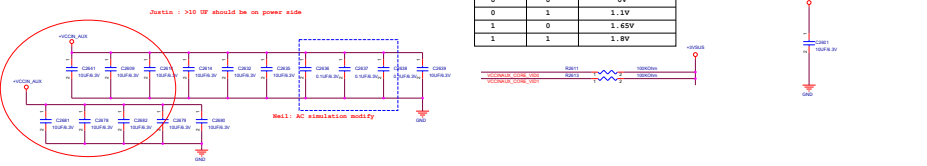
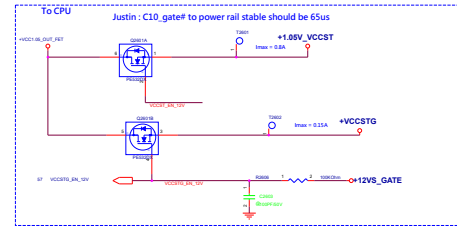
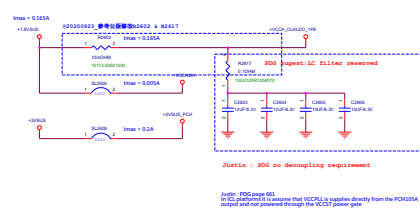
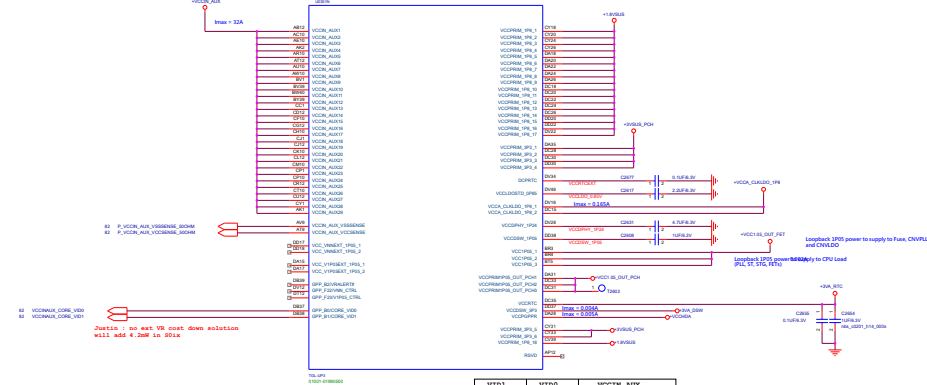
C

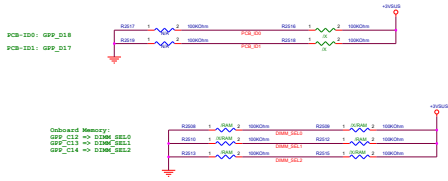
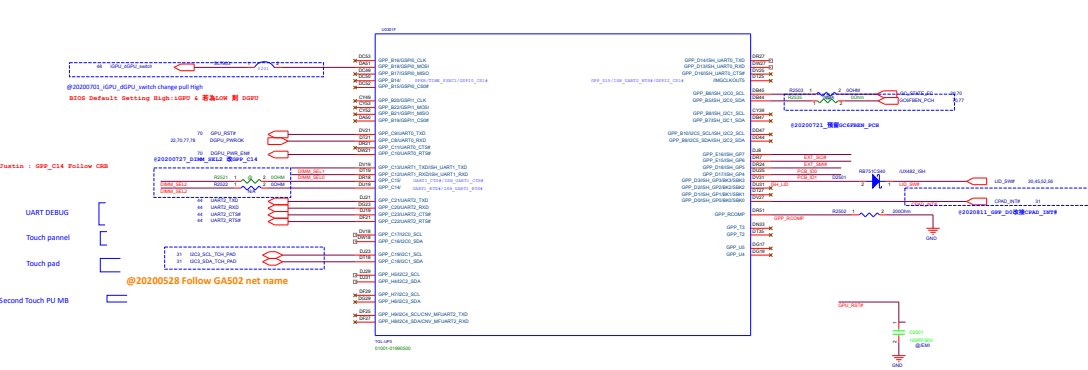
Dept.: **NB1-RD3EE2**

Engineer: **EE**

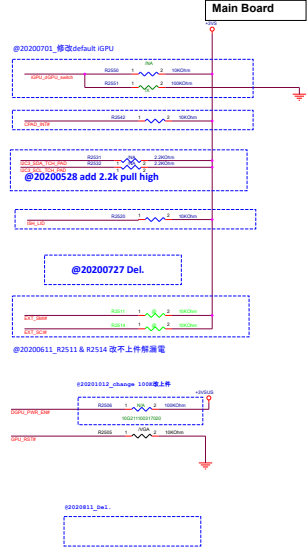
Date: **Wednesday, March 17, 2021**

Sheet **24** of **102**





MEMORY DOWN Table			D12M_SEL4			Key Part List		
			R2514	R2513	R2512			
			2	1	0			
03012-00070200	R2513 目前線路	Samung 1Gb	0	0	0	主料: R2509 / R2512 / R2513 不上料: R2509 / R2512 / R2513		
			0	0	1			
03012-00040600	R2514	MICRO 8Gb	0	1	0	主料: R2508 / R2512 / R2513 不上料: R2508 / R2512 / R2513		
03012-00040700	R2512	Samung 8Gb	0	1	1	主料: R2509 / R2512 / R2513 不上料: R2508 / R2512 / R2513		
			1	0	0			
03012-00070300	R2511	Bynisk 16Gb	1	0	1	主料: R2509 / R2510 / R2515 不上料: R2508 / R2512 / R2513		
			1	1	1			



Project Name

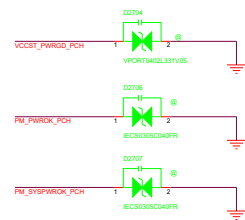
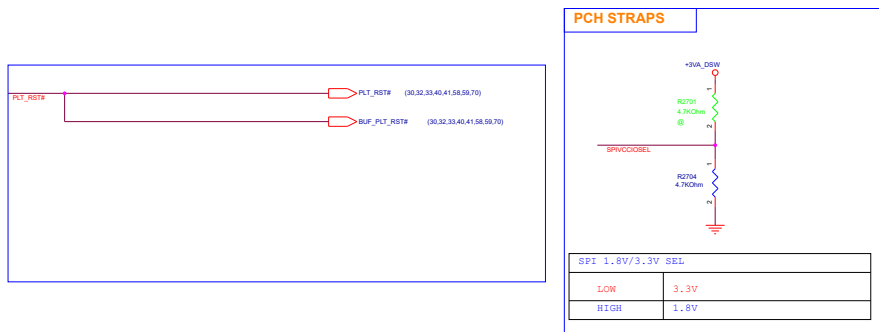
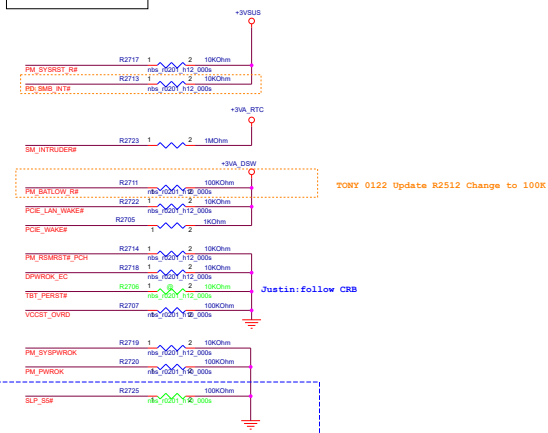
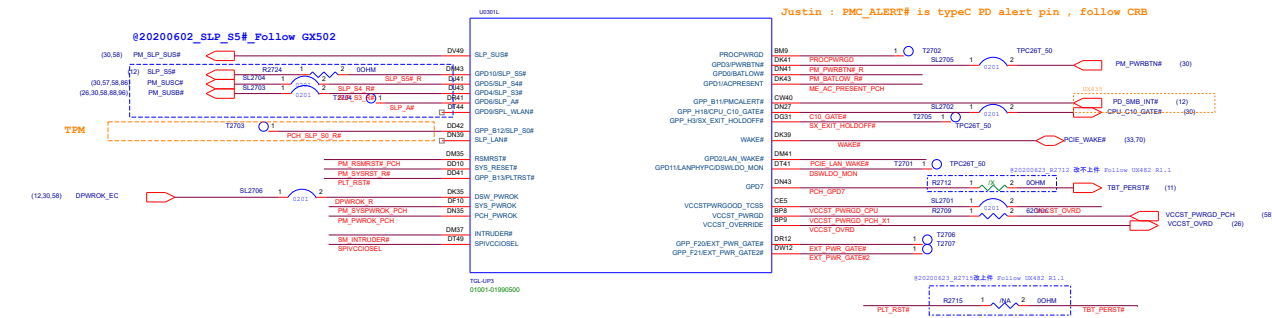
Project Name

Project Name

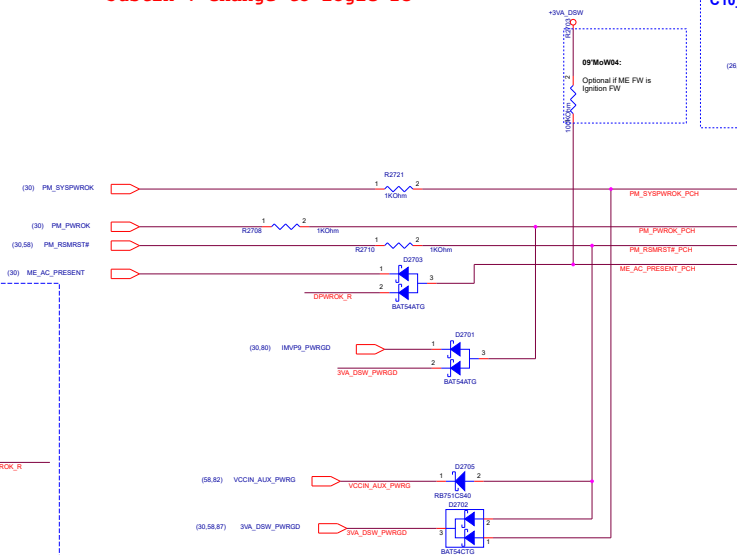
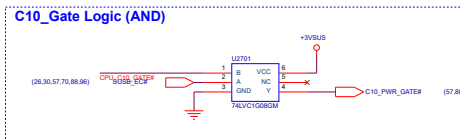
Project Name

Project Name

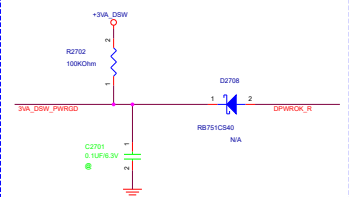
Project Name



Justin : change to logic IC




Change to UX334FL
Andy1 Shih 0114



Power failure solution (S0-->G3,S5-->G3):

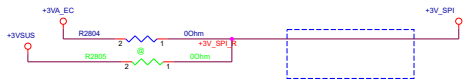
Justin : take DSW PWROK low on emergency power loss, it must also take RSMRST# low at the same time

<Variant Name>

		Project Name		Rev
		UX482		R0.1
Title : Test Point				
Size	Dept.: NB1-RD3EE2		Engineer:	EE
B				
Date: Wednesday, March 17, 2021			Sheet	29 of 102

System Management Interface

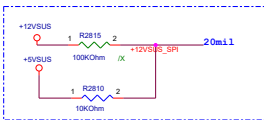
Justin : for PD platform using +3VA_EC to avoid dead battery issue.



SPI0 2-Load(1 Flash and 1TPM)
EC G3 flash sharing with Wire-OR Topology
Justin :Follow DG 6.12.3.2

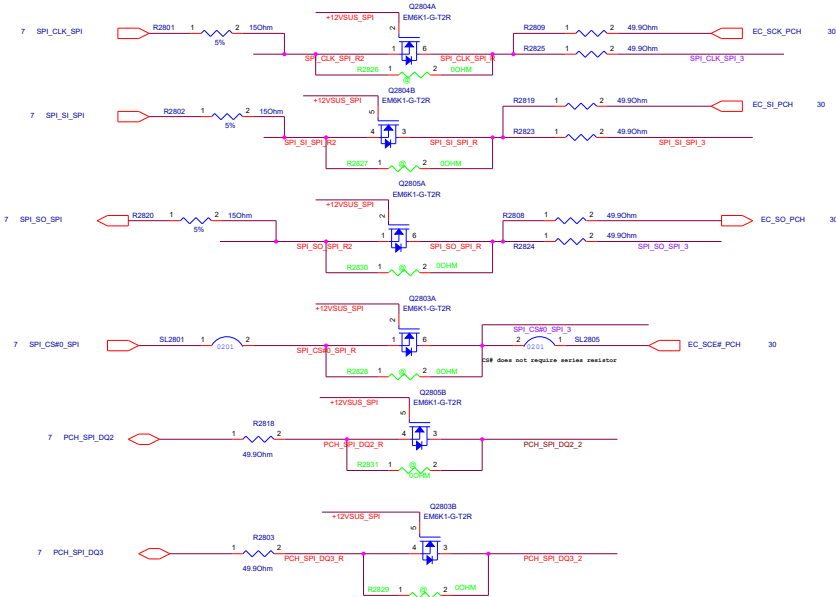
Note. No TPM : R1 22 ohm
R2 75 ohm
R3 22 ohm
R4 X

R1.3 PD project should use isolation avoid SPI leakage



@20200611 新增R2810 Pull 5VSUS
並將R2815改不上件,解漏電

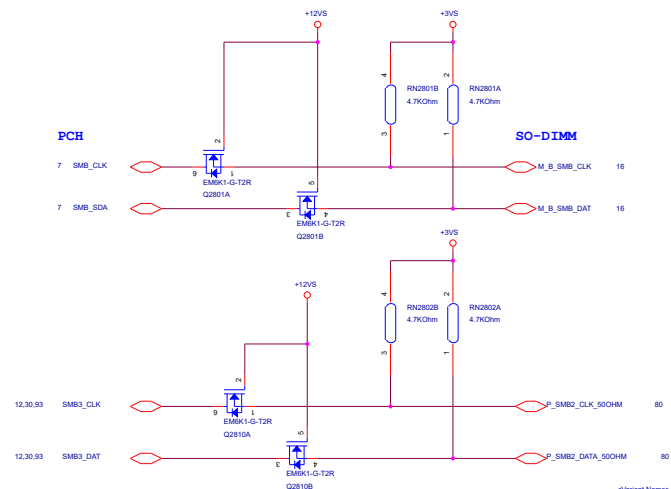
PCH,TPM Side



EC,SPI ROM Side

@20200602 Remove SMB_CLK to AMP & NVVDD CLK Switch

SMBus Interface



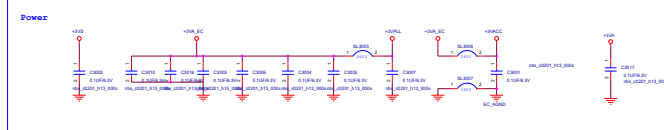
<Variant Name>

Only 3V Tolerance
 GPB[0,1,2,3,4,5,6]
 GPB[3,4,5,6,7]
 GPB[0,4,6,7]
 GPF[4,7]
 GPF[6,7]
 GPF[10,7]
 GPF[10,7]

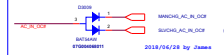
Can be adjusted to
 Open-Drain for port:

GPAD-GPA3
 GPB0-GPB7
 GPD0-GPD7
 GPE0-GPE7
 GPF0-GPF7
 GPG0-GPG6
 GP30-GP35

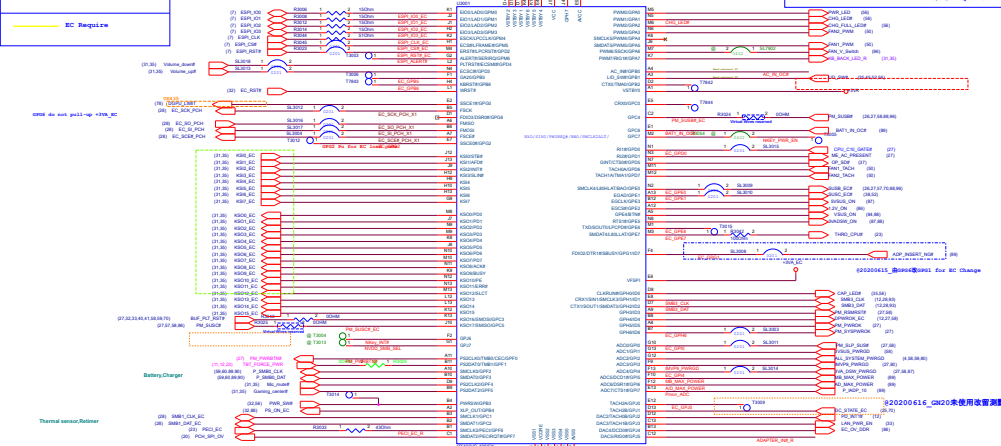
EC ReguLow



Justin : ICL ESP1 support 1.8V only.



2018/10/28 By Joma

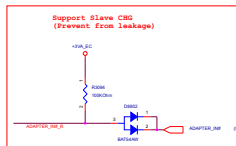


06037-00370200
 20200515 更新料號

BGA 7.1*7.1*0.97

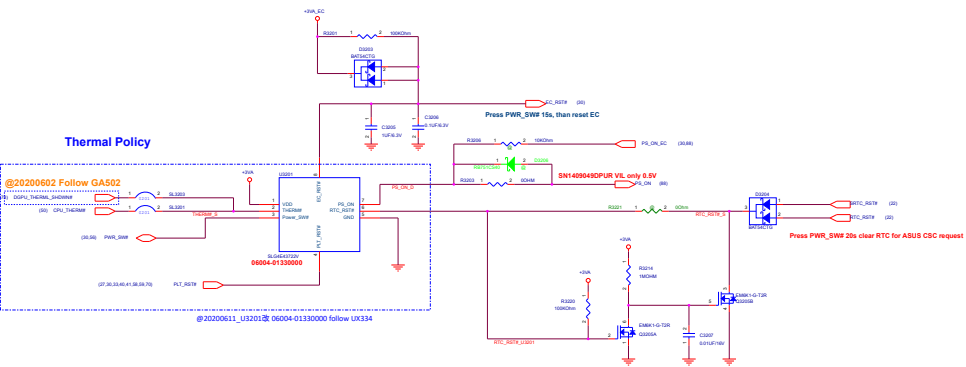
EMI request

IT5125VG-128/CX (128KB) (06037-00370000) ?
 IT5125VG-192/CX (192KB) (06037-00370200)

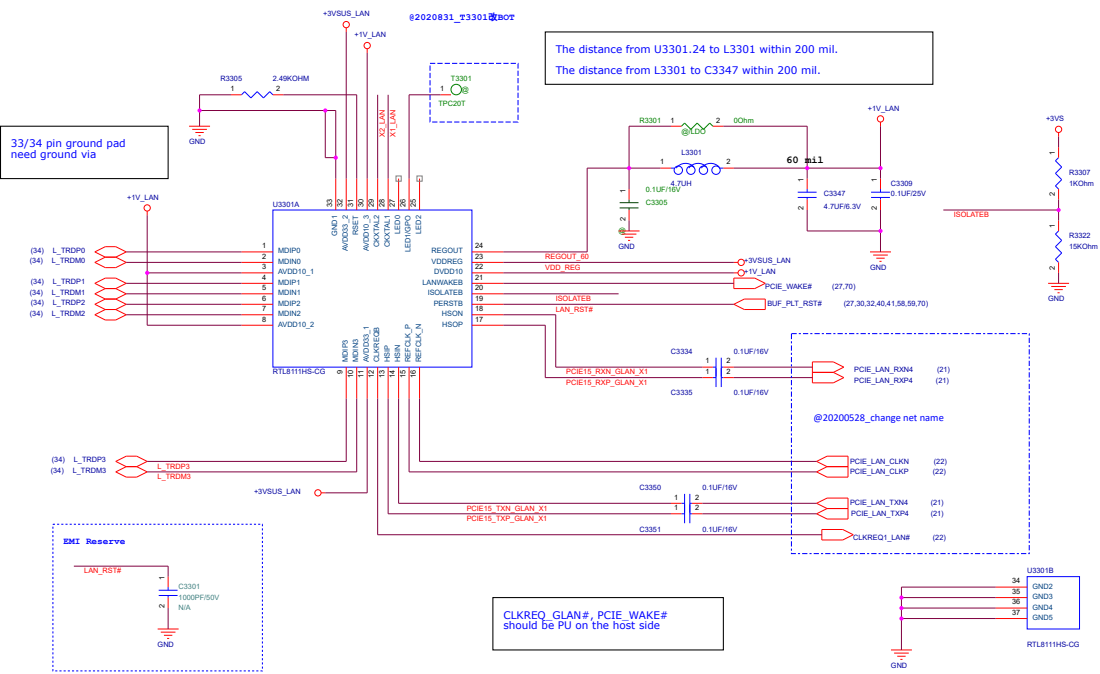


PM_RDMUTE remove pull down @ EC side

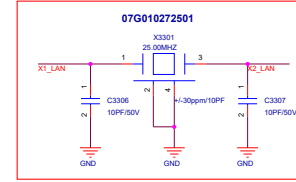




Main Board



@20200615_換回較常用XTAL 但體積較大 for GA502 & GX502

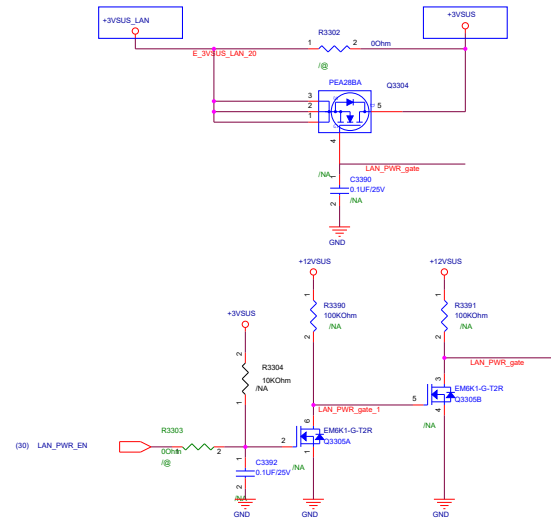


X3301: 25MHZ +/-30ppm/10pF (3225)

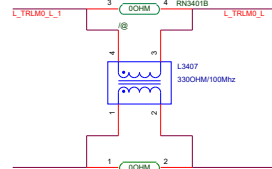
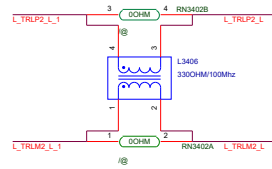
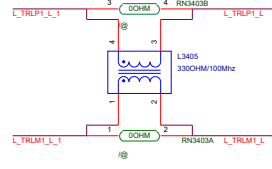
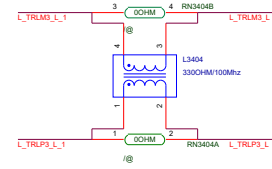
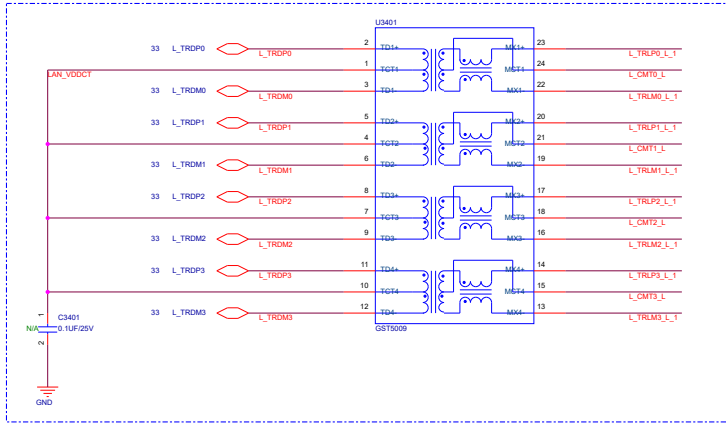
1st: P/N:07G010272501 TXC/7V25000011

2nd: P/N:07G010952500 HOSONIC/E3FB25

Realtek suggests 3V_LAN raise time >1ms

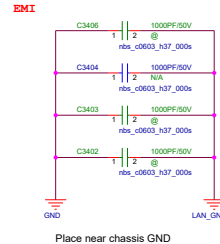
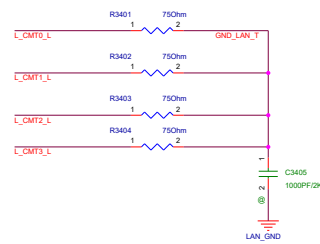
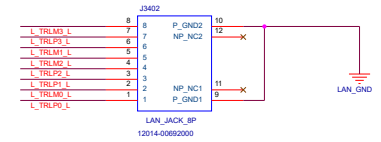


@20200702_Rf要求修改連線順序



Main Board

LAN Connector

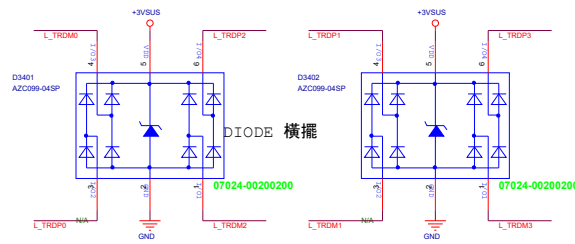


D3401,D3402 ESD Diode

1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G

2nd Source: P/N:07024-00710000 NXP/PUSB2X4D

GND_LAN_T 上禁止加任何零件

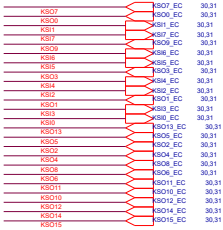
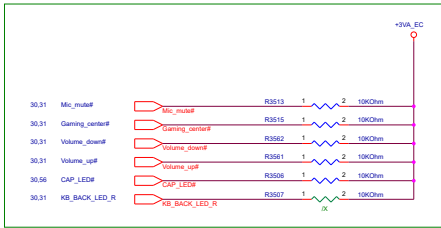
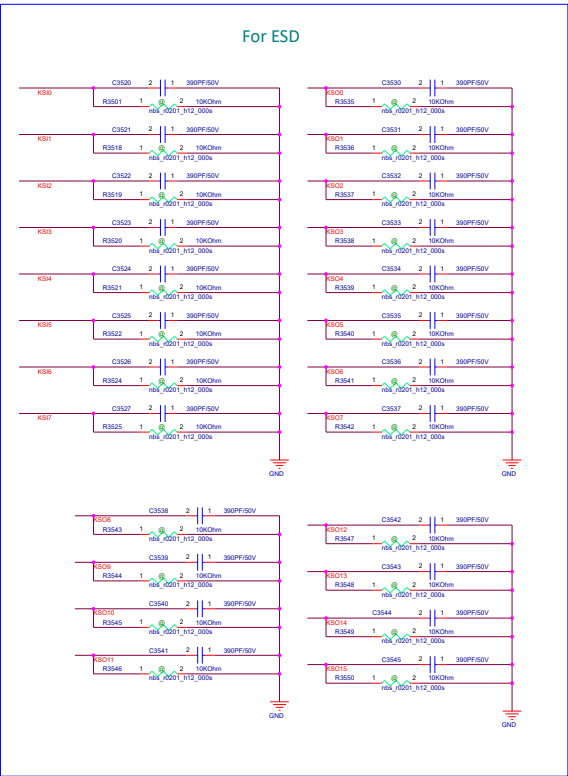


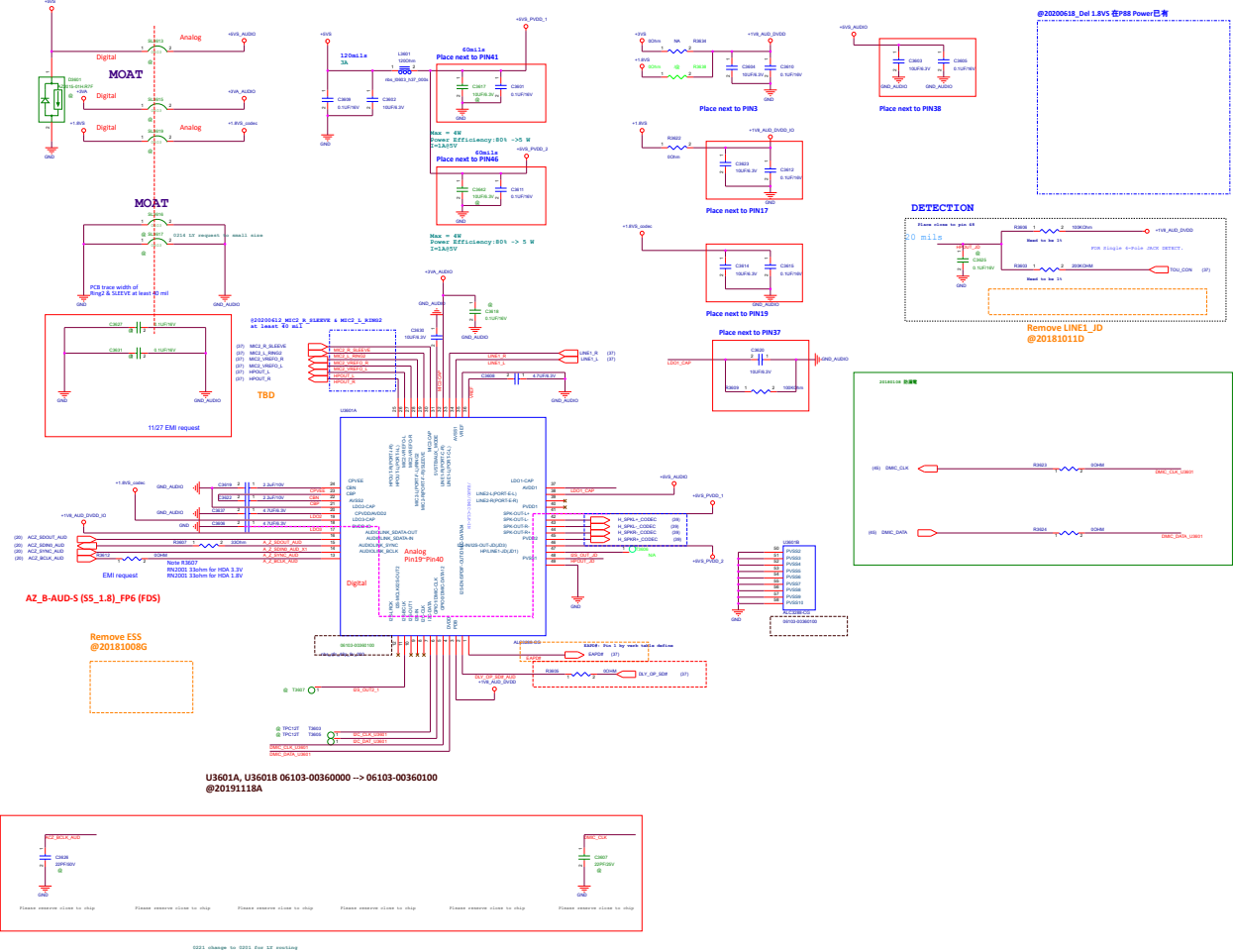
D3401,D3402 ESD Diode

1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G

2nd Source: P/N:07024-00710000 NXP/PUSB2X4D

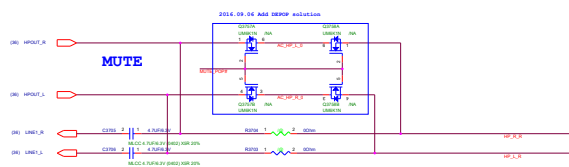
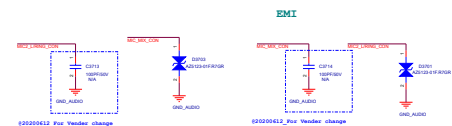
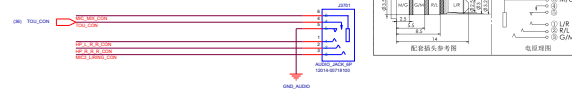
Pull up





A_{in} GND / GND

The diagram shows three capacitors connected in parallel between the input signal line (A_{in}) and ground (GND). Each capacitor is labeled with its value (0.1uF) and pin numbers (2 and 1). The ground connection is labeled GND_AUDIO and GND.



Tong 0122 D3962 Change to 07000408011 (D3435)

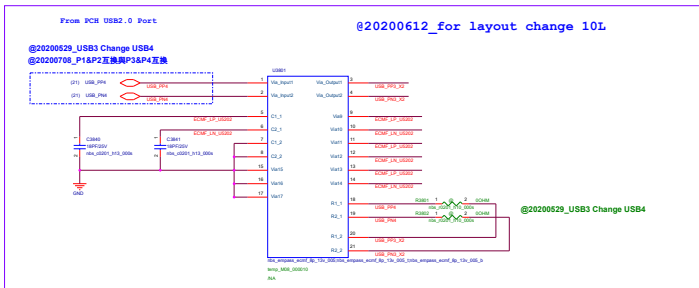
MUTE CONTROL new solution for 1.8V ADA BUG 0318

ADA Bug Fix Rev. 03/08

USB3.1 Direct



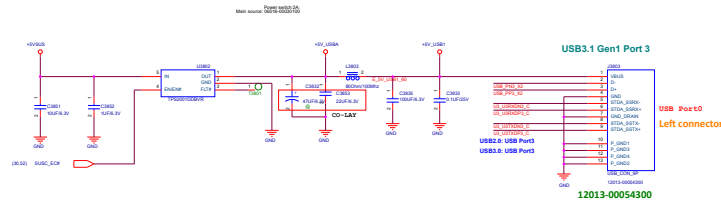
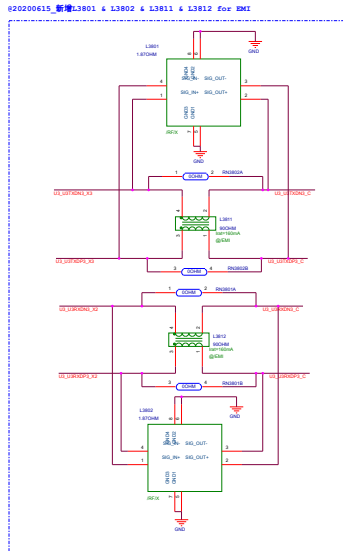
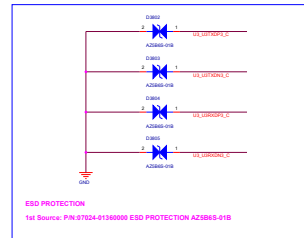
USB2.0 EMI-Protection With ECMF(PCB 1.05mm_10Layer)



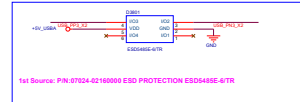
Note :

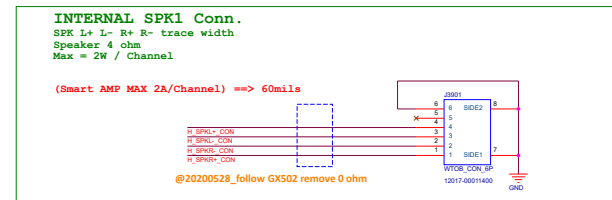
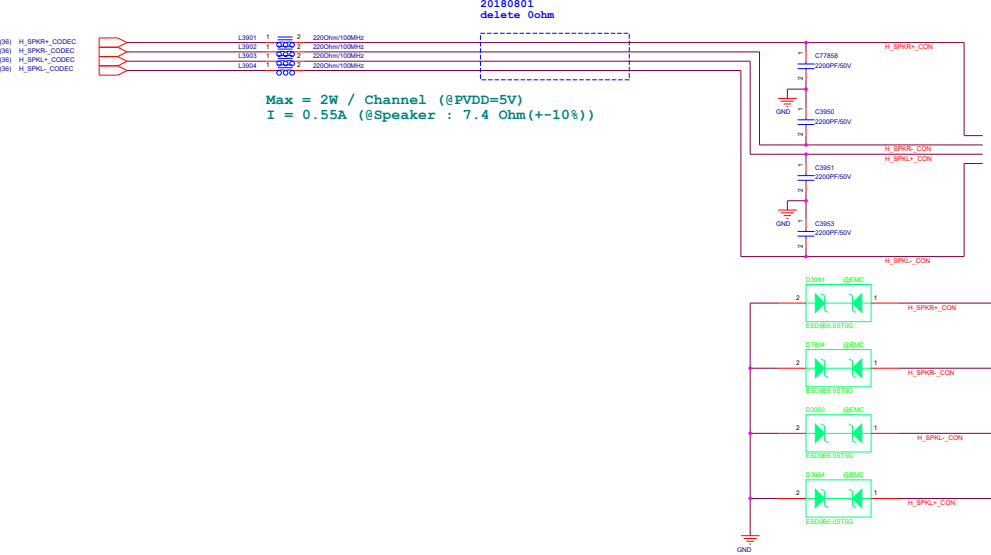
1. This part & symbol only apply for standard PCB stack-up listed in datasheet appendix I
Please check your project must matching the thickness , DF and DK value of PCB every layer
2. C5209&C5210 must be replaced with 18pF 0201 capacitors and the tolerance of capacitance value is 5%
3. Pin7 & Pin8 & Pin11 & Pin12 must be connected to system ground
4. Pin13 to Pin16 are floated in regular scheme

USB3.0 ESD-Protection

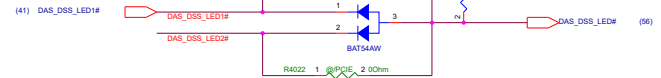


USB2.0 ESD-Protection

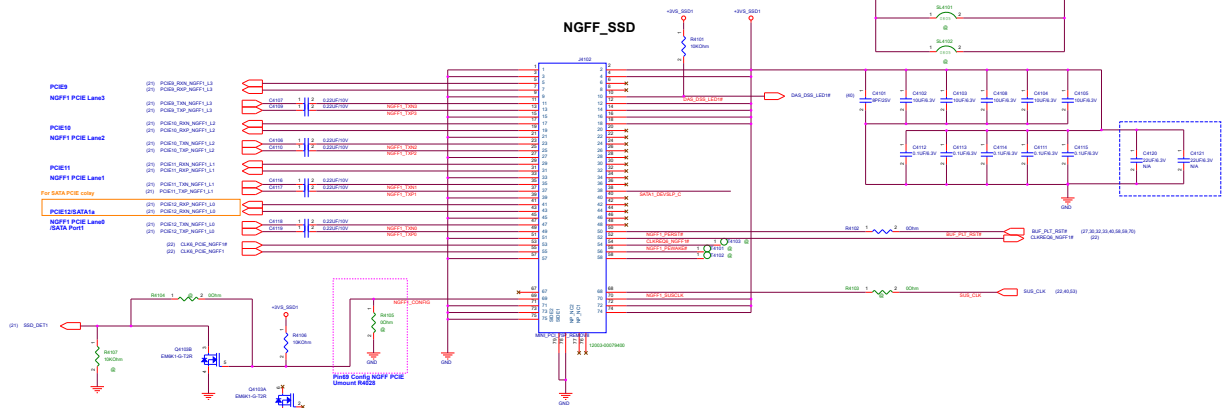




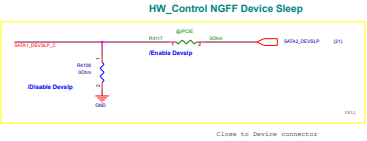
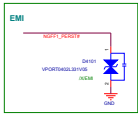
@20200702_layout空間關係調高更換J4001 & H4002



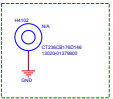
NGFF_SSD



Option	NGFF1_CONFIG	SSD_DET1
PCIe SSD	1	0
SATA SSD	0	1





12003-00079400



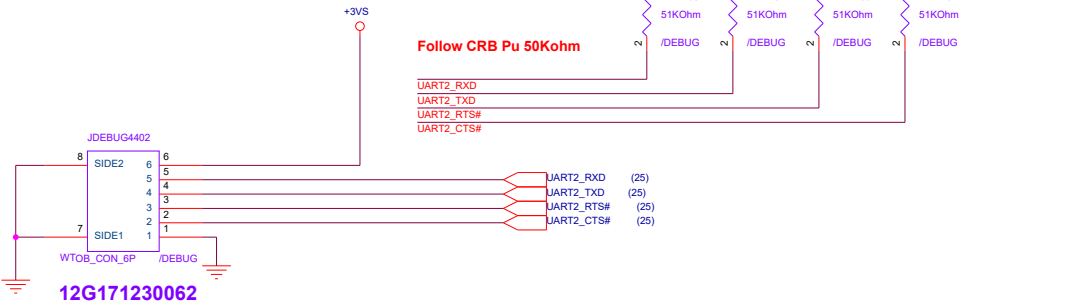
13020-01379900

<Variant Name>

		Title : XDD_HDD & ODD CON	
ASUSTeK COMPUTER		Engineer: EE	
Size A	Project Name GX502GX		Rev 1.0
Date: Wednesday, March 17, 2021		Sheet 42 of 102	


		Project Name		Rev
		UX482		R0.1
Title : CB-****				
Size	Dept.:		Engineer:	
C	NB1-RD3EE2		EE	
Date: Wednesday, March 17, 2021			Sheet	43 of 102


UART Debug card



Jigboard4 debug guide
DIP SW to 0000 : BIOS Flash
DIP SW to 0010 : Keyboard CONN Port80
DIP SW to 1000 : SMBUS CONN Port80 & BIOS DUMP (by Postcode monitor)

<Core Design>

		Title : DEBUG_LPC	
ASUSTeK COMPUTER		Engineer: EE	
Size B	Project Name GX502GX		Rev 1.0
Date: Wednesday, March 17, 2021		Sheet 44 of 102	

		Project Name UX482		Rev R0.1
Title : CRT_D-Sub				
Size B	Dept.: NB1-RD3EE2		Engineer:	EE
Date: Wednesday, March 17, 2021			Sheet	46 of 102

~Variant Name~

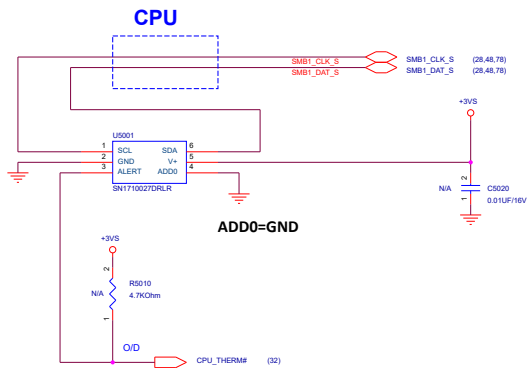
		Project Name UX482		Rev R0.1
Title : Display Port				
Size C	Dept.: MSI-PD3002		Engineer:	EE
Date: Wednesday, March 17, 2021			Sheet	47 of 102

Thermal Sensor : SN170027

ALERT/SDA/SCL: Open-drain output; pullup resistor 5Kohm

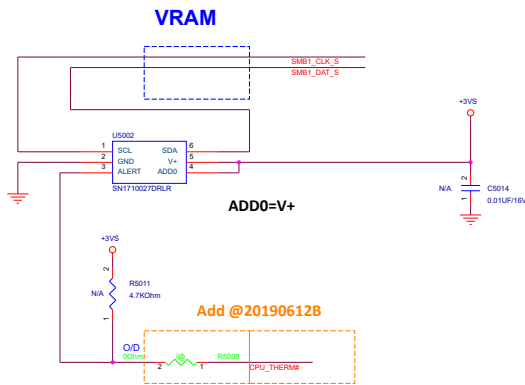
Pin function Supply voltage.: 1.62 V to 3.6 V

@20200728_Modify thermal Del. 0 ohm



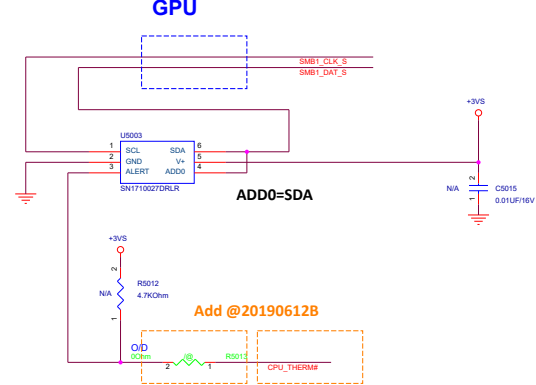
Near CPU

SMBUS addr=10010000 (90)



Near VRAM

SMBUS addr=10010001 (91)

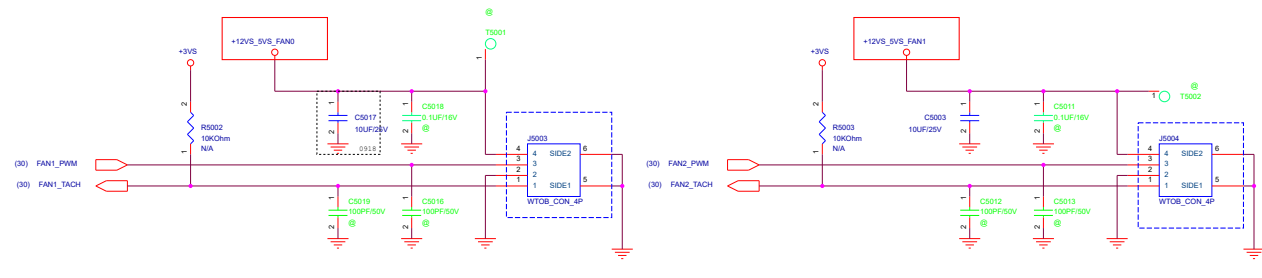


Near GPU

SMBUS addr=10010010 (92)

CPU&GPU FAN

Note : connector and power are by project design

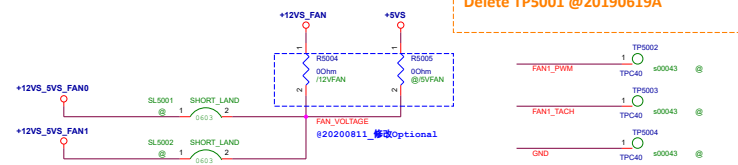


@20200810_Change to 12017-00330300

@20200810_Change to 12017-00330300

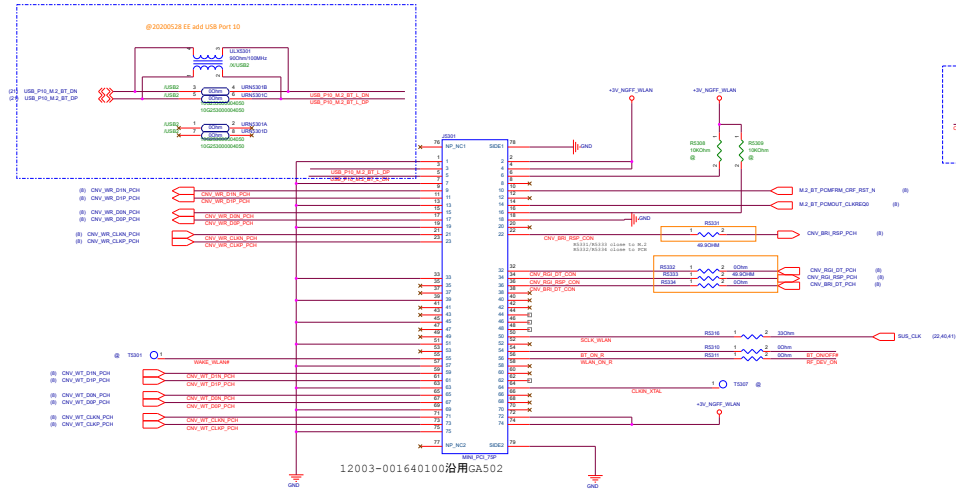
ADD0: Address select. Connect to GND, SDA, SCL, or V+

DEVICE TWO-WIRE ADDRESS	ADD0 PIN CONNECTION	Output
1001000 90	Ground	CPU
1001001 91	V+	VRAM
1001010 92	SDA	GPU
1001011 93	SCL	



Delete TP5001 @20190619A

<Core Design>



[CNV Mode Select] CNV AGI DT PCR
An external pull-up of pull-down is required.
0 = Integrated CNVi enable.
1 = Integrated CNVi disable.

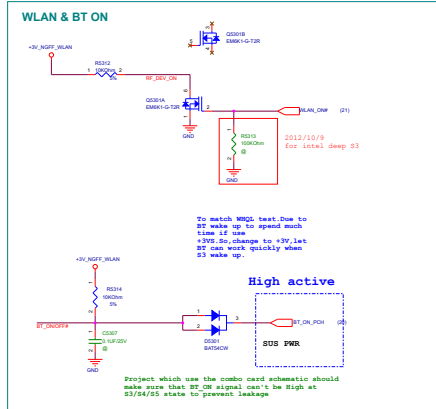
```
[Intel FAE]
RGI_DT has an automatic detect CNVi mechanism,
please do not use external PD.
The CRF has an internal strong 1K PD already.
Do not leave this pin float.
if CNVi is not used, it still need a 20K ohm PU.
```

WLAN PWR_+3V_NGFF_WLAN (Non-ISCT)
Support ASUS Open Cloud Computing (AOConnect)
WLAN PWR to +3VSUS



Remove WLAN and LAN power switch circuit
2019.11.19

@20200611_del WLAN_Wake# Control for RF

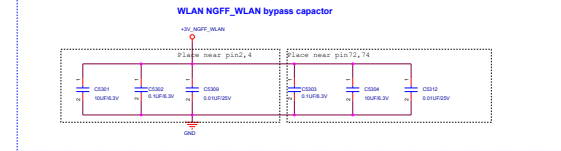


Screw Hole

13020-01371400
5 013 5762 073 85L-8L 1-5N-5MO



20200707 Rex 新增





Project Name

UX482

Rev

R0.1

Title : **G-Sensor**

Size

B

Dept.: **NB1-RD3EE2**

Engineer: **EE**

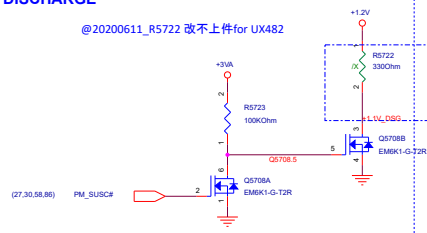
Date: **Wednesday, March 17, 2021**

Sheet **54** of **102**

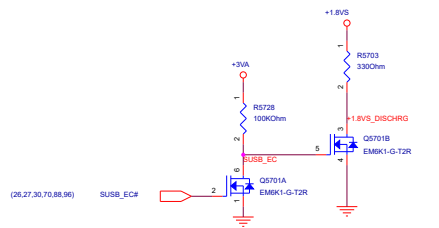
Justin : Removed no used Discharge circuit
1.8V, VCCIO, +5VS load switch already build in 180~260 ohm discharge function

+1.1V DISCHARGE

@20200611_R5722 改不上件for UX482



@20200611_R5702 改不上件for UX482



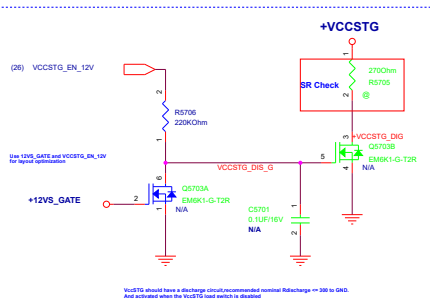
+VCCSTG

(26) VCCSTG_EN_12V

Use 12VS_GATE and VCCSTG_EN_12V for board optimization

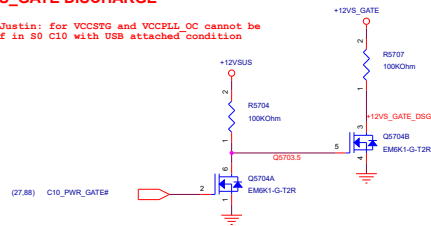
+12VS_GATE

VCCSTG should have a discharge circuit recommended nominal Discharge => 300 to 0V.
And activated when the VccSTG load switch is disabled



+12VS_GATE DISCHARGE

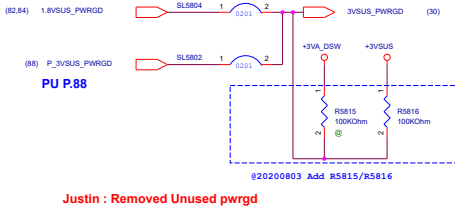
R1.1B Justin: for VCCSTG and VCCPLL_OC cannot be cut off in S0 C10 with USB attached condition



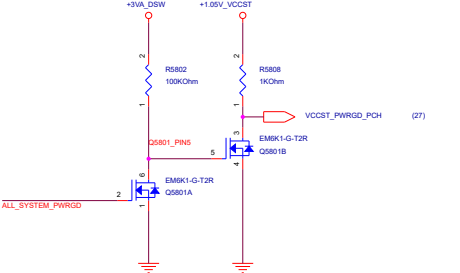
<<Variant Name>>

ASUS		Project Name	Rev
Title : DSG_Discharge			R0.1
Size	Dept.: N81-RD3EE2	Engineer: EE	
Date: Wednesday, March 17, 2021	Sheet	57	of 102

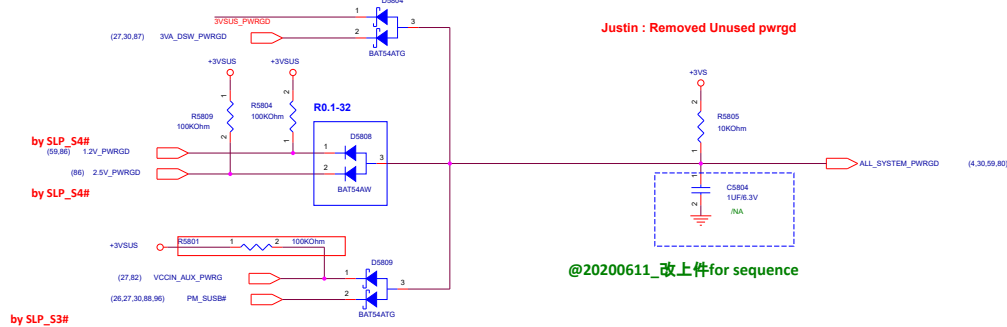
3VSUS_PWRGD



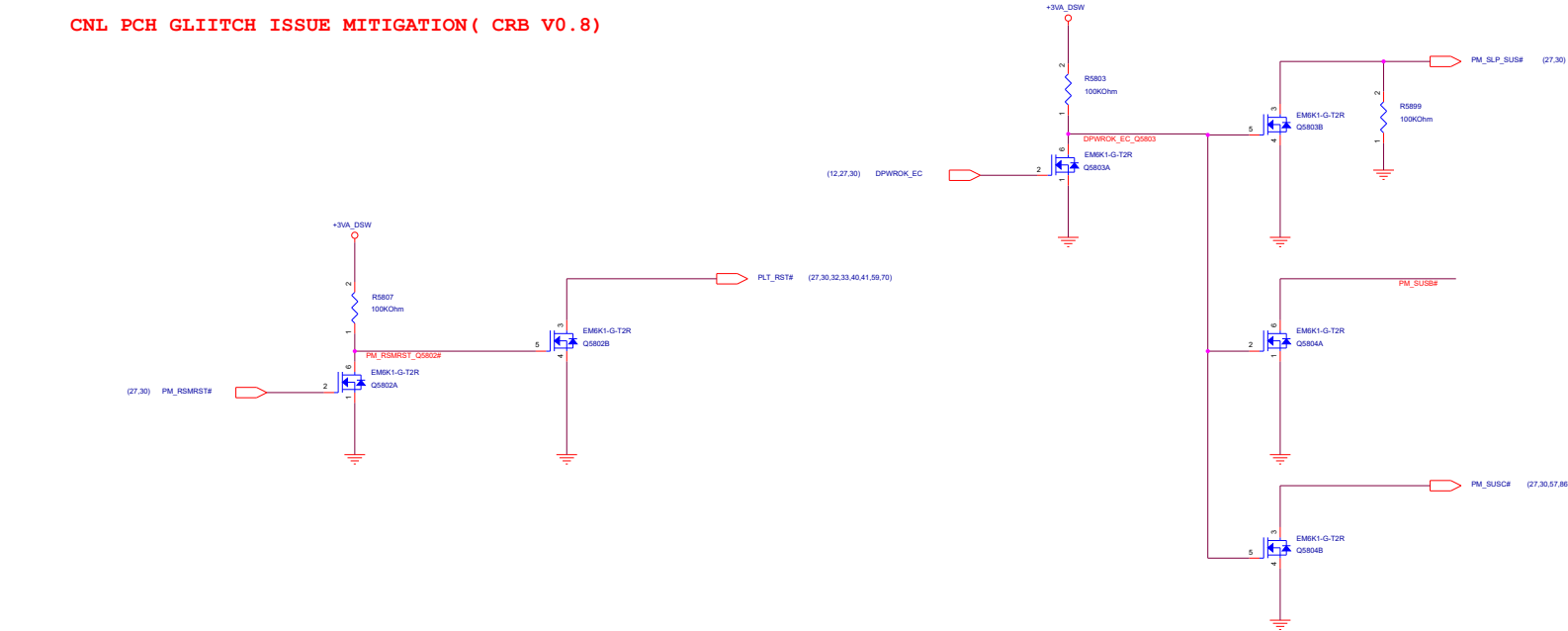
VCCST_PWRGD



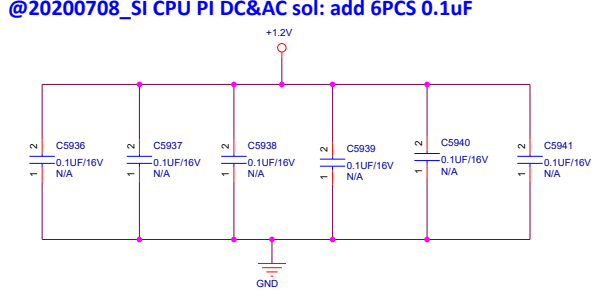
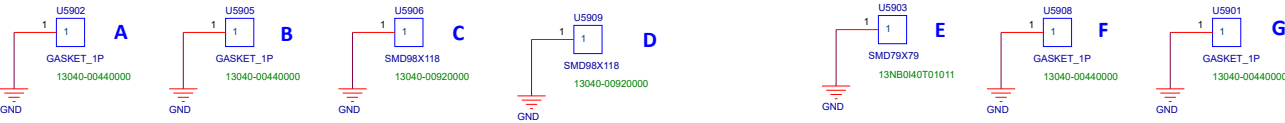
ALL_SYS_PWRGD



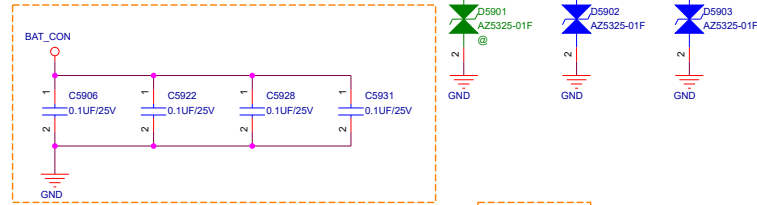
CNL_PCH_GLIITCH ISSUE MITIGATION(CRB V0.8)



@20201021_Modify SMT EMI GASKET

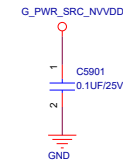
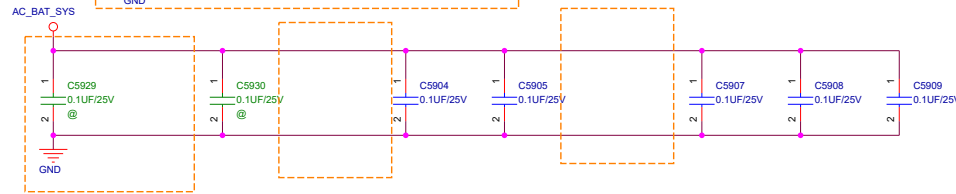
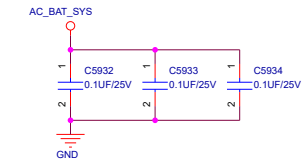


EMI request @20181026A

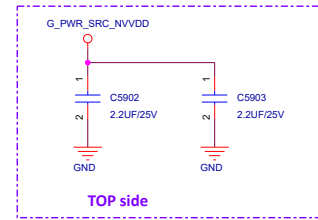


將U6904, U6908(改裸銅), U6905(改裸銅) 移除 @20181122C

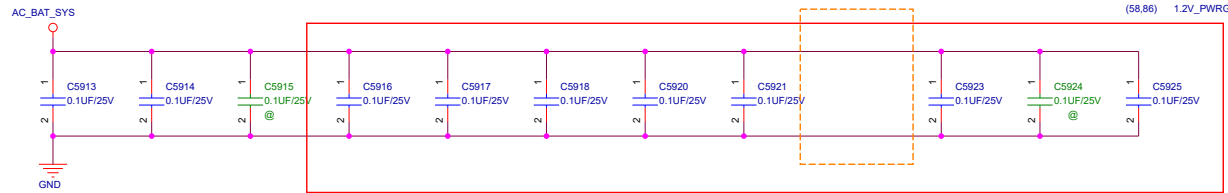
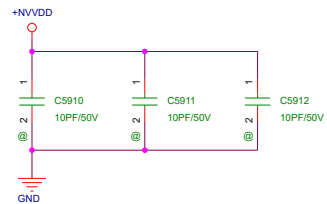
2017/04/05 EMI



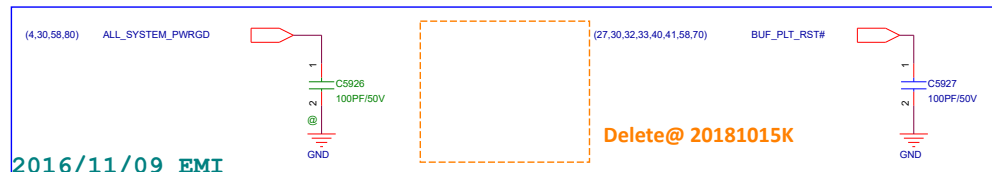
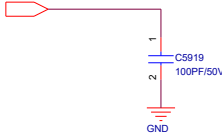
4/2 for EMI



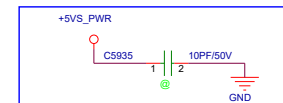
2016/07/27 EMI



GX501VI 1.1H



2016/11/09 EMI



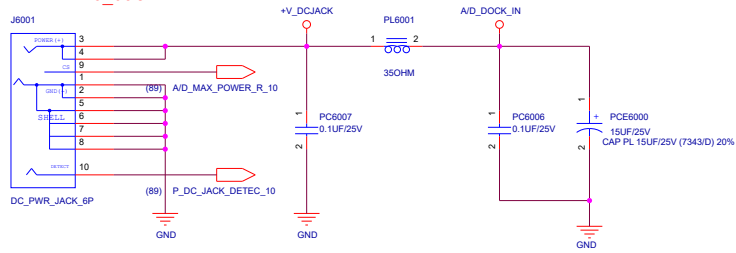
<Core Design> 2017.05.02 EMI Reserve

ASUS		Title : OTH_EMI	
ASUSTek COMPUTER		Engineer: EE	
Size B	Project Name	GX502GX	
Date: Wednesday, March 17, 2021	Sheet	59 of 102	Rev 1.0

DC-IN Connector

DC Jack使用請詢用River_Hsu

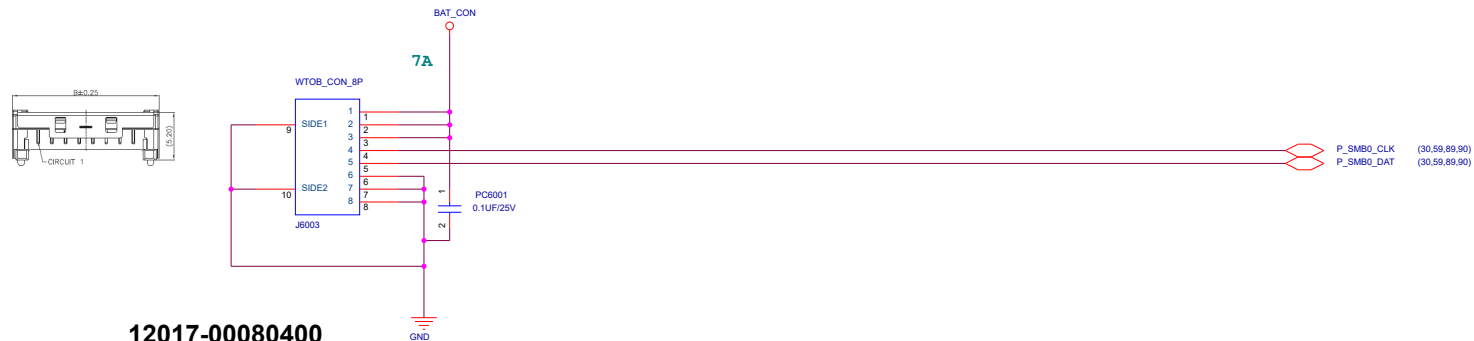
New 6 Phi 4 Pin DC_Jack



J6001	3.4CH	1.55CH
	12033-00020200	12033-00020300

CHIP Cap (H=2.1)

Battery Connector



12017-00080400

Note: Battery Connector 正確性與BAT1_IN_OC#是否預留!



Project Name

UX482

Rev

R0.1

Title :


Size


C

Dept.: NB1-RD3EE2**Engineer:** EE


Date: Wednesday, March 17, 2021

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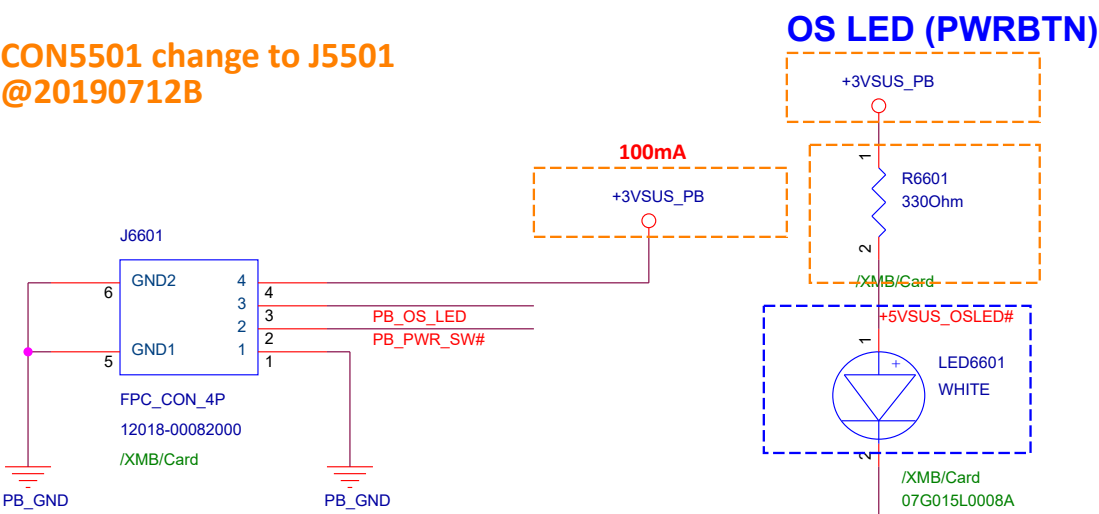
		Title : I/O board(1-1)_CR_RTS5139	
ASUSTeK COMPUTER		Engineer: EE	
Size A	Project Name GX502GX		Rev R1.2
Date: Wednesday, March 17, 2021		Sheet 62 of 102	

		Project Name		Rev
		UX482		R0.1
Title : NFC				
Size				
C	Dept.:	NB1-RD3EE2	Engineer:	EE
Date: Wednesday, March 17, 2021			Sheet	63 of 102

BOM

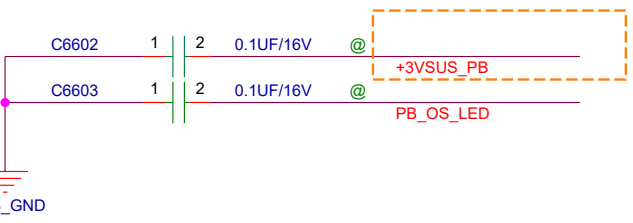
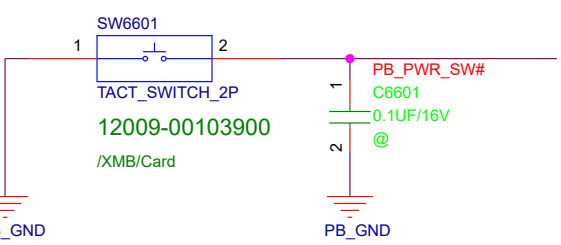
		Project Name	Rev
		UX482	RD.1
Title :			
Size	Dept.:		Engineer:
B	NB1-RD3EE2		EE
Date:	Wednesday, March 17, 2021	Sheet	64 of 102

CON5501 change to J5501
@20190712B

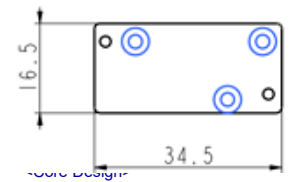
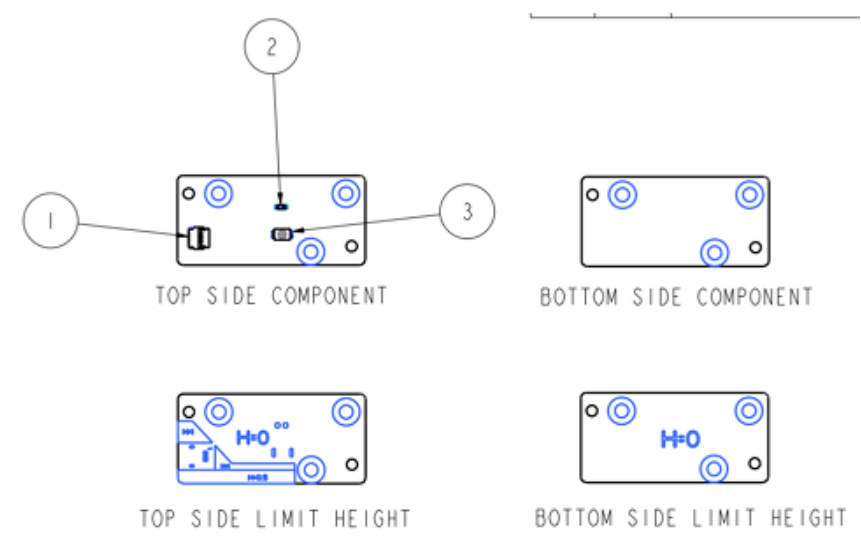
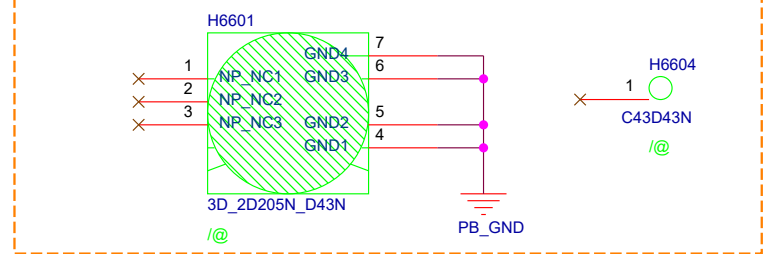


@20200813 Power Key LED 换白光 07G015L0008A
+5VSUS_PB --> +3VSUS_PB
R5510 750 OHM --> 330 OHM
@20190708A

POWER button




Change @20181026B



		Title : IO Con. to MB	
ASUSTeK COMPUTER		Engineer: EE	
Size A	Project Name GX502GX		Rev 1.0
Date: Wednesday, March 17, 2021		Sheet 66	of 102

Del.@20201215

<Variant Name>

		Title : KBC_KB & TP	
ASUSTeK COMPUTER		Engineer: EE	
Size C	Project Name GM501		Rev R1.0
Date: Wednesday, March 17, 2021		Sheet 67 of 102	



Project Name

UX482

Rev

R0.1

Title :

Size

B

Dept.: NB1-RD3EE2**Engineer:** EE

Date: Wednesday, March 17, 2021

Sheet

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<Variant Name>

Title

<Title>

Size

A

Document Number

G512LI

Rev

R1.0

Date:

Wednesday, March 17, 2021

Sheet

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of

102

<Variant Name>

Title

<Title>

Size

A

Document Number

G512LI

Rev

R1.0

Date:

Wednesday, March 17, 2021

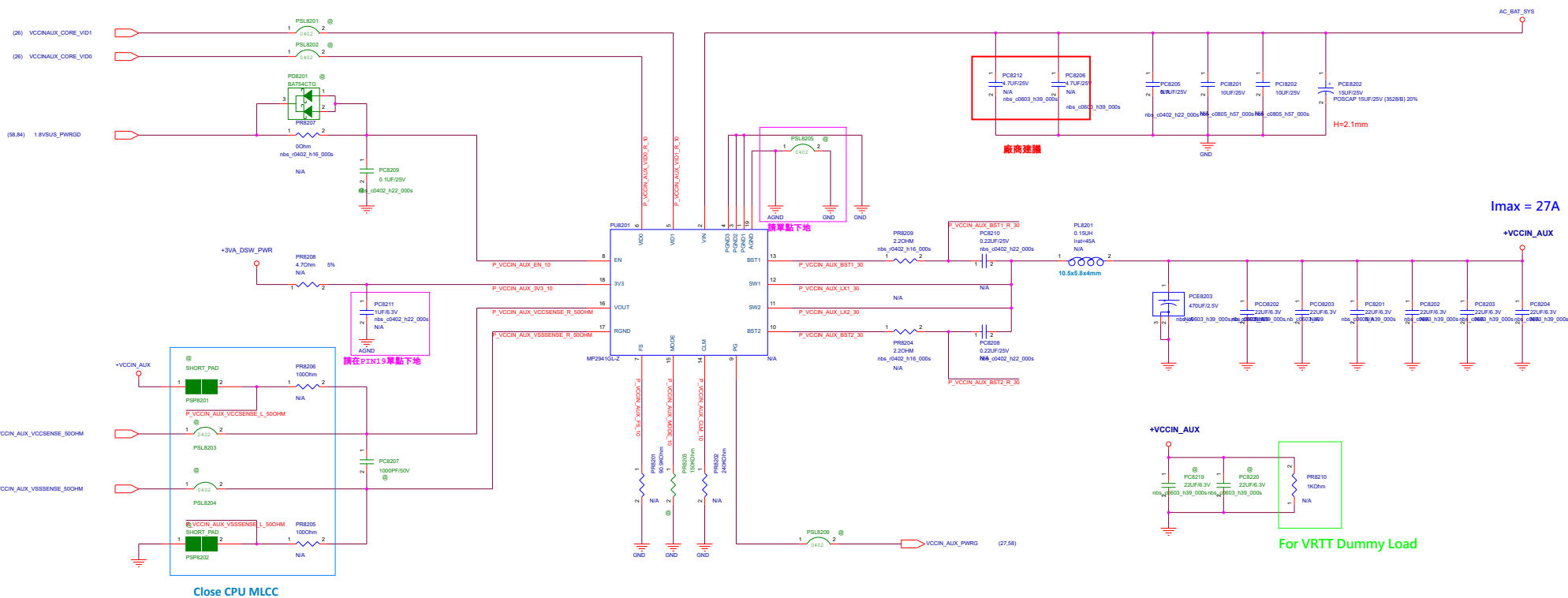
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TGL IMVP9 (3) Power [For CPU]



<Variant Name>



Project Name

UX482

Rev

R0.1

Title : **POWER**

Size

Custom

Dept.: **NB1-RD3EE2**

Engineer: **Andy**

Date: **Wednesday, March 17, 2021**

Sheet

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of

102

<Variant Name>



Project Name

UX482

Rev

R0.1

Title : **POWER**

Size

Custom

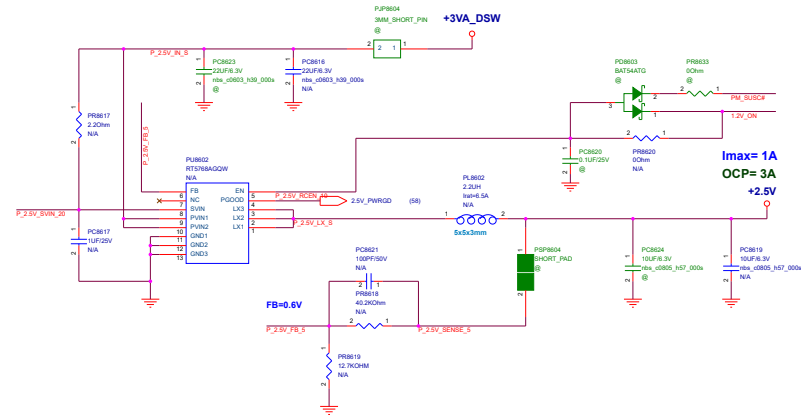
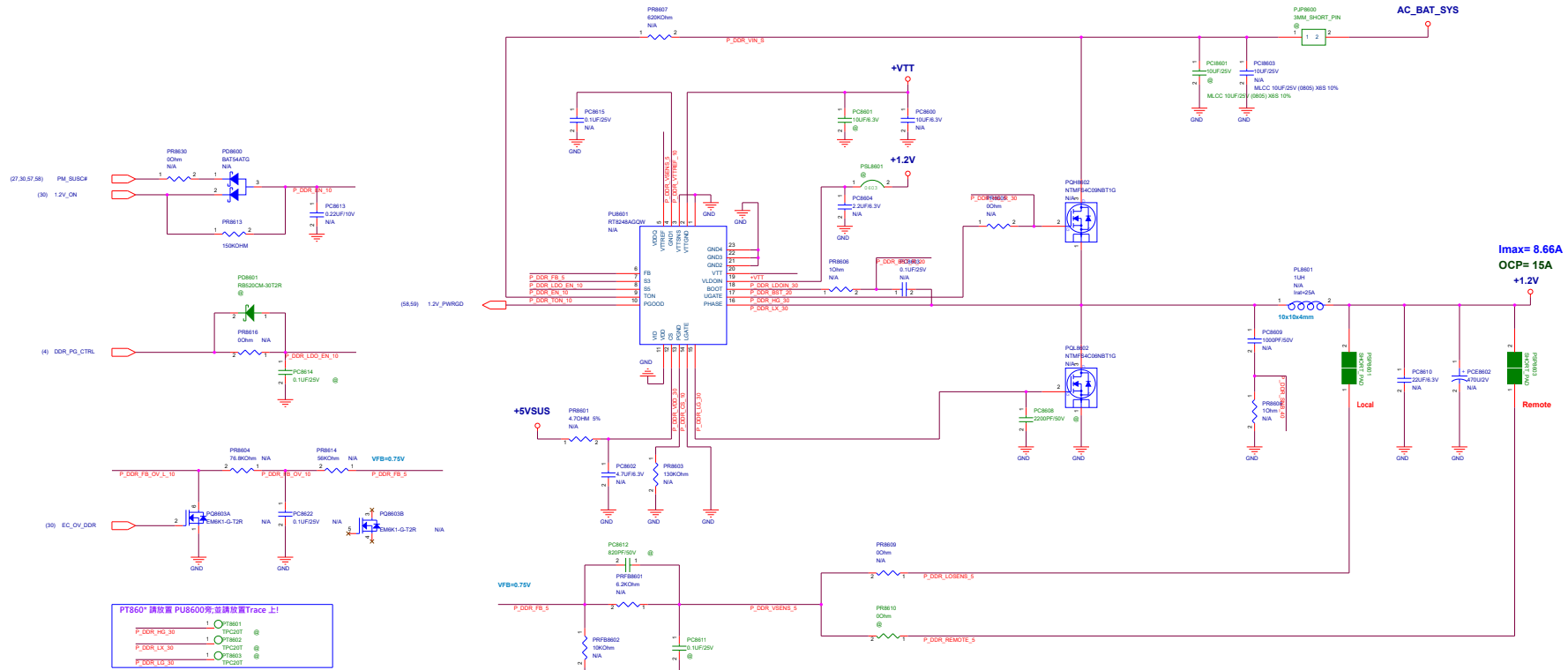
Dept.: **NB1-RD3EE2**

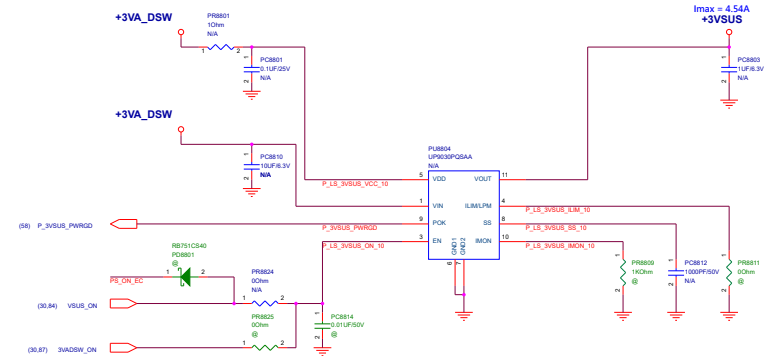
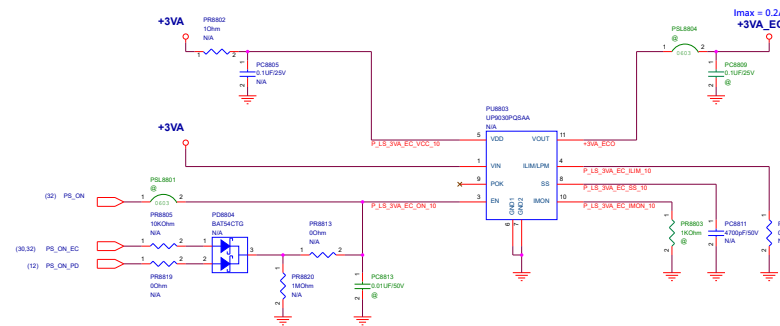
Engineer: **Andy**

Date: **Wednesday, March 17, 2021**

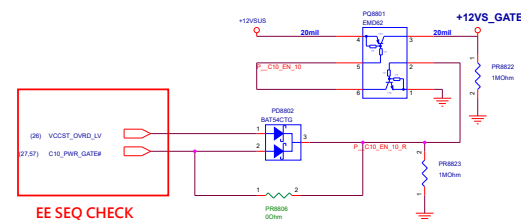
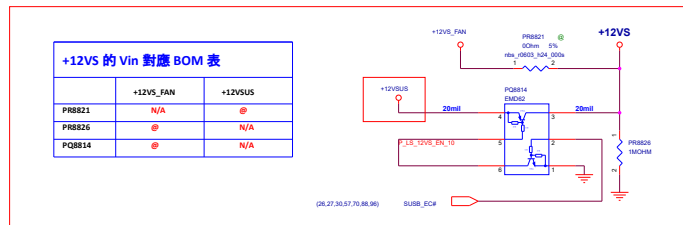
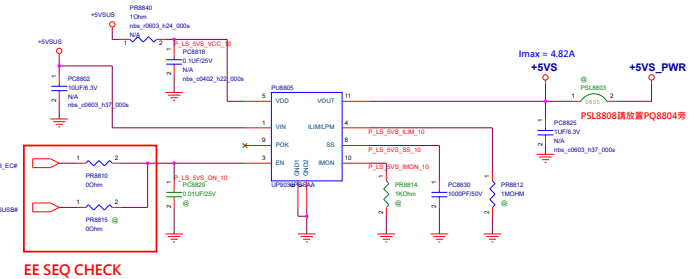
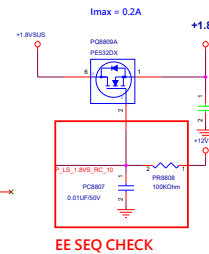
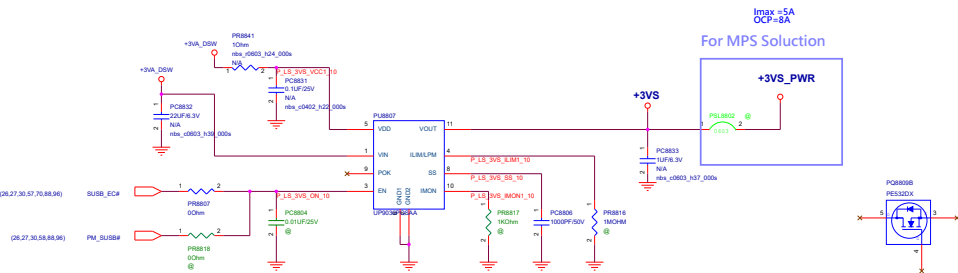
Sheet **85** of **102**

+1.2V / +VTT / +VTT [For Memory]





uP9030 ILIM/LPM Setting 對應表		
ILIM PIN	LPM (C10)	LIMIT Current
GND	Off	3A
1M to GND	Off	5A
Roat/VDD	On	8A



BOM



Adaptor select			
		4 Series	5 Series
FR8901		10m	5m
FR8936			
14E CONNECTOR (FR8936-01)	0.4V	45W	120W
31.6E CONNECTOR (FR8936-02)	0.8V	50W	150W
54E CONNECTOR (FR8936-03)	1.2V	180W	180W
82.1E CONNECTOR (FR8936-04)	1.6V	65W	230W
150E CONNECTOR (FR8936-05)	2.0V	NA	270W
270E CONNECTOR (FR8936-06)	2.4V	90W	200W
560E CONNECTOR (FR8936-07)	2.8V	120W	240W

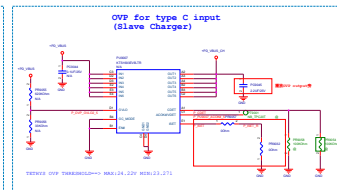
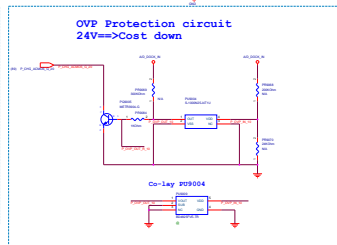
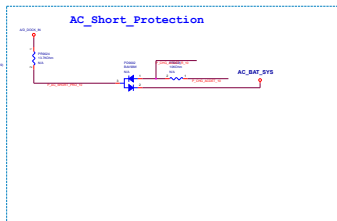
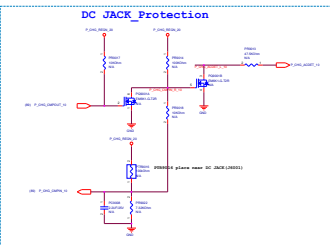
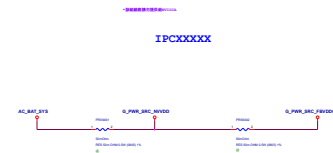
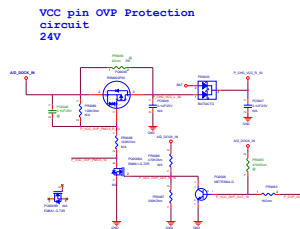
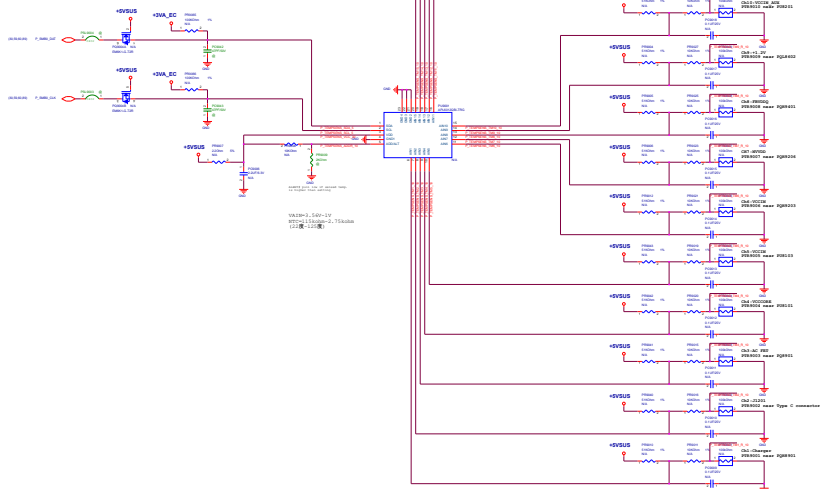


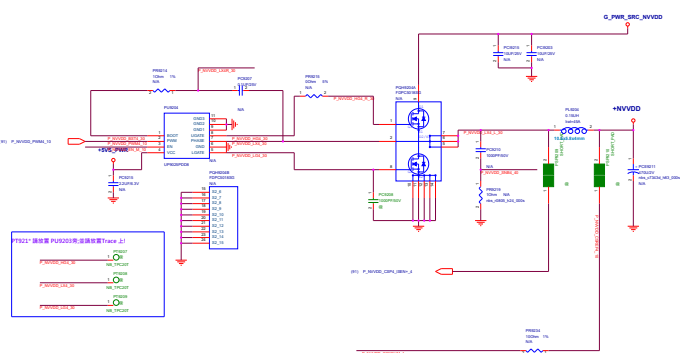
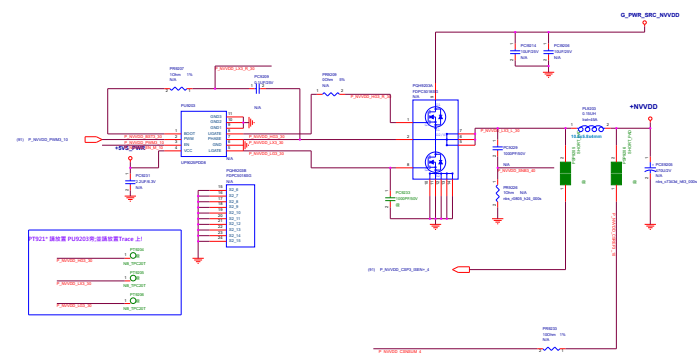
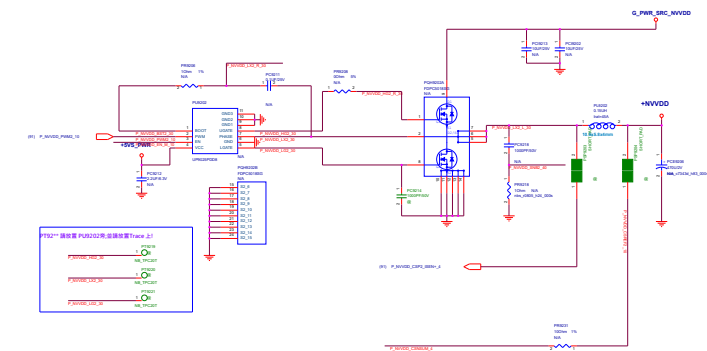
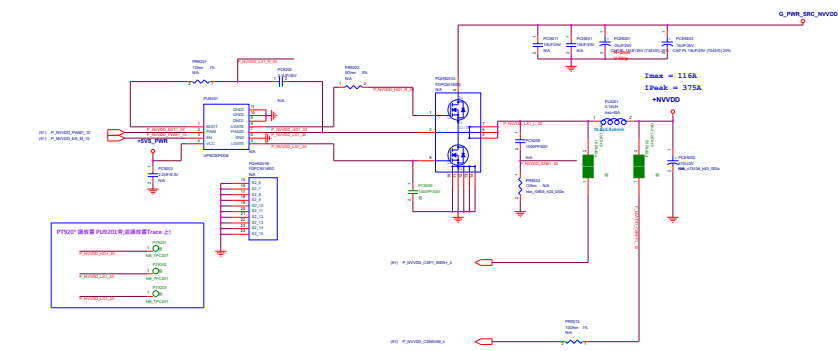
Address Selection Table

Chip Select	Bank	Address	Device
CS0	0	0x00000000	0x00000000
CS1	1	0x00000000	0x00000000
CS2	2	0x00000000	0x00000000
CS3	3	0x00000000	0x00000000
CS4	4	0x00000000	0x00000000
CS5	5	0x00000000	0x00000000
CS6	6	0x00000000	0x00000000
CS7	7	0x00000000	0x00000000
CS8	8	0x00000000	0x00000000
CS9	9	0x00000000	0x00000000
CS10	10	0x00000000	0x00000000
CS11	11	0x00000000	0x00000000
CS12	12	0x00000000	0x00000000
CS13	13	0x00000000	0x00000000
CS14	14	0x00000000	0x00000000
CS15	15	0x00000000	0x00000000

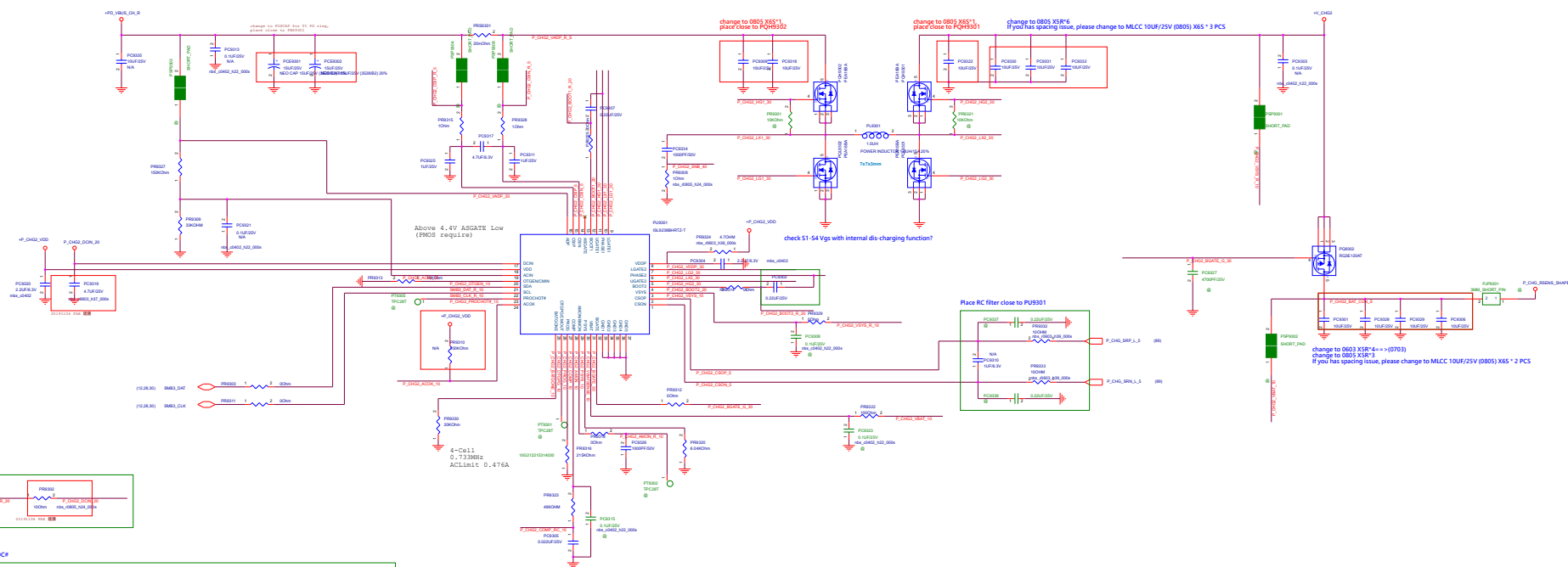
Register Address

Bank	Address	Device
0	0x00000000	0x00000000
1	0x00000000	0x00000000
2	0x00000000	0x00000000
3	0x00000000	0x00000000
4	0x00000000	0x00000000
5	0x00000000	0x00000000
6	0x00000000	0x00000000
7	0x00000000	0x00000000
8	0x00000000	0x00000000
9	0x00000000	0x00000000
10	0x00000000	0x00000000
11	0x00000000	0x00000000
12	0x00000000	0x00000000
13	0x00000000	0x00000000
14	0x00000000	0x00000000
15	0x00000000	0x00000000





Charger ISL9238 (NVDC)

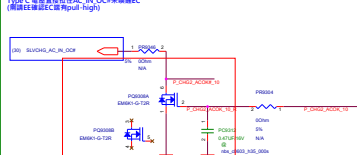


Check operating current(light /havey load-->15mA)



For power state S5, wake-up EC by PD plug-in AC_IN_OC#

Type C 電壓直接拉往AC, IN, OC#來喚醒EC
(與環境喚醒EC一樣pull-high)



PT940* 請放置 PU9401旁;並請放置Trace 上



<Variant Name>



Project Name

UX482

Rev

R0.1

Title : **POWER**

Size

Custom

Dept.: **NB1-RD3EE2**

Engineer: **Andy**

Date: **Wednesday, March 17, 2021**

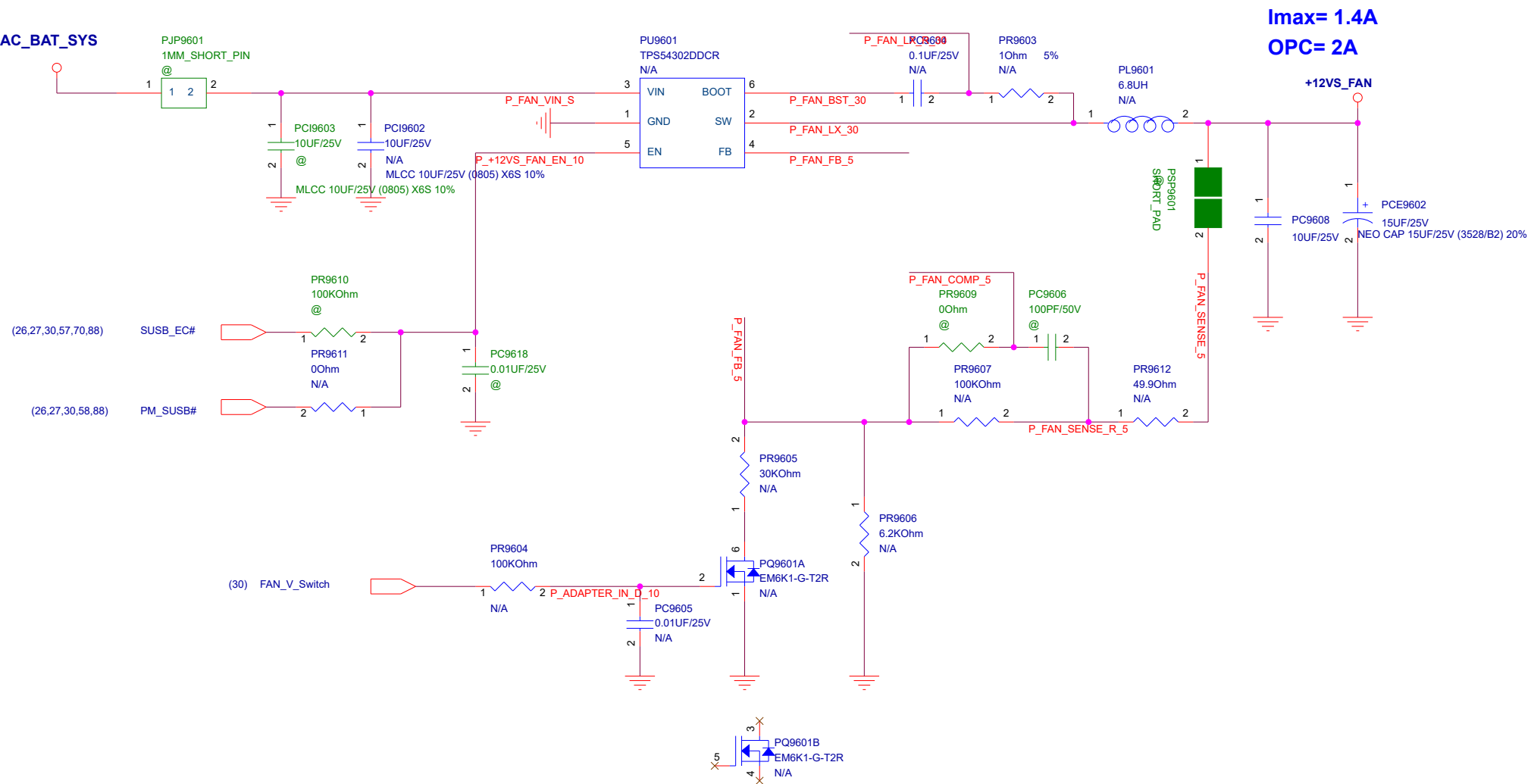
Sheet

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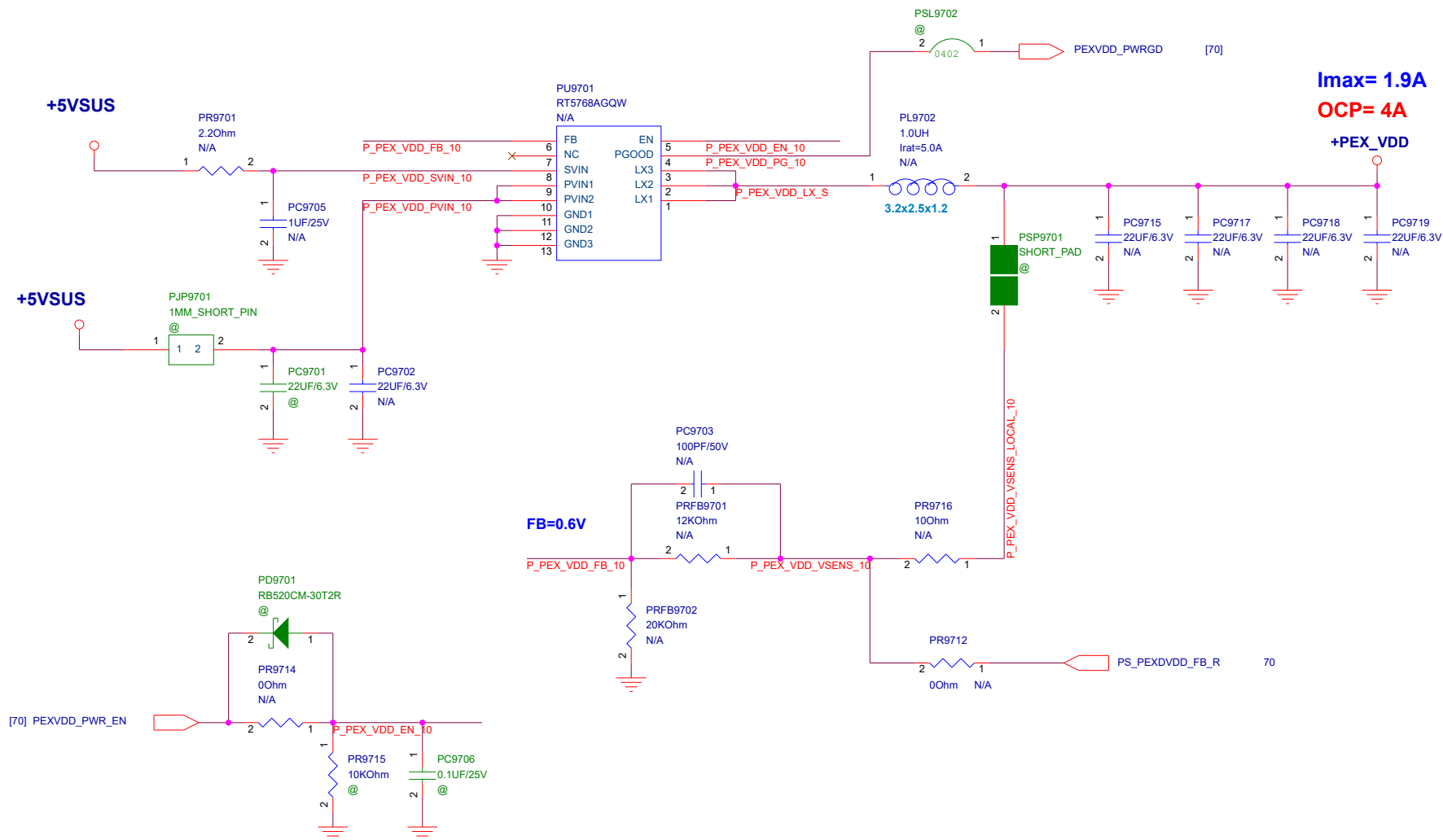
+12VS_FAN [For FAN]




<Variant Name>

		Project Name Project Name	Rev R1.0
Title : PW_+12VS_FAN			
Size A4	Dept.: NB Power team		Engineer: Power RD
Date: Wednesday, March 17, 2021		Sheet 96 of 102	

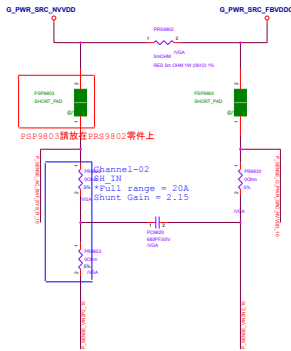
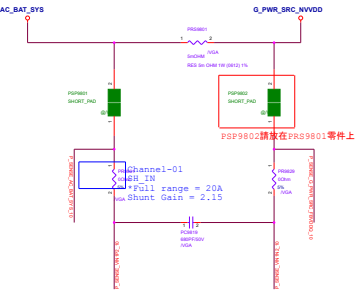
PEX_VDD [For GPU]



<Core Design>

		Project Name Project Name	Rev R1.0
Title : PW_+PEX_VDD			
Size A4	Dept.: NB Power team	Engineer: Power RD	
Date: Wednesday, March 17, 2021		Sheet 97 of 102	

OVR-M GEN1 UPI



Channel-01

BS_IN

*Full range = 19V

Bus Gain = 6.4514m

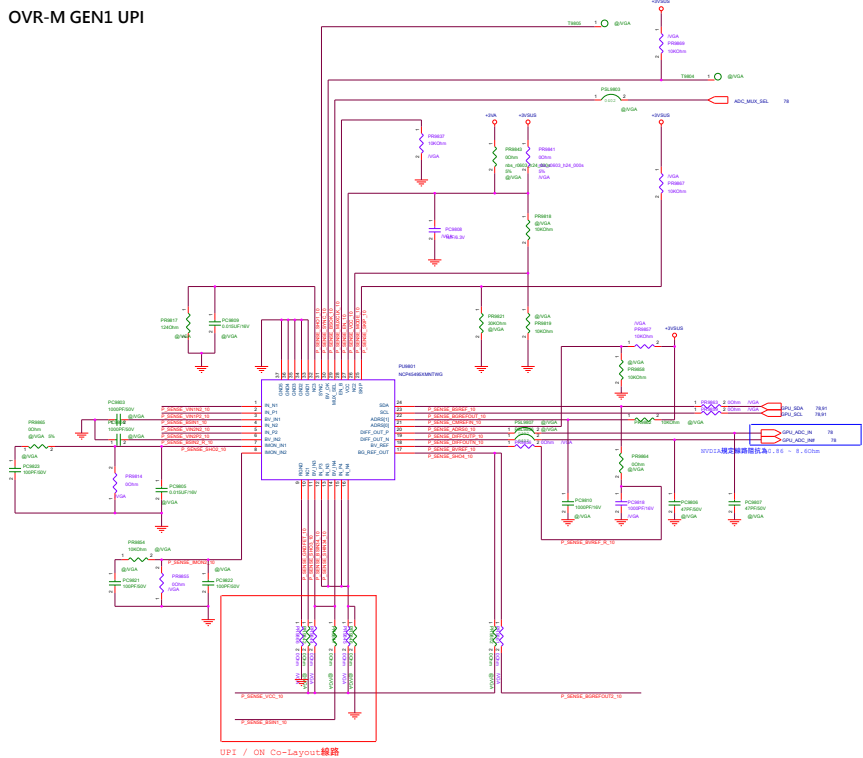
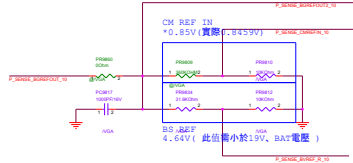
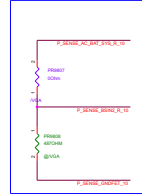


Channel-02

BS_IN

*Full range = 19V

Bus Gain = 6.4514m

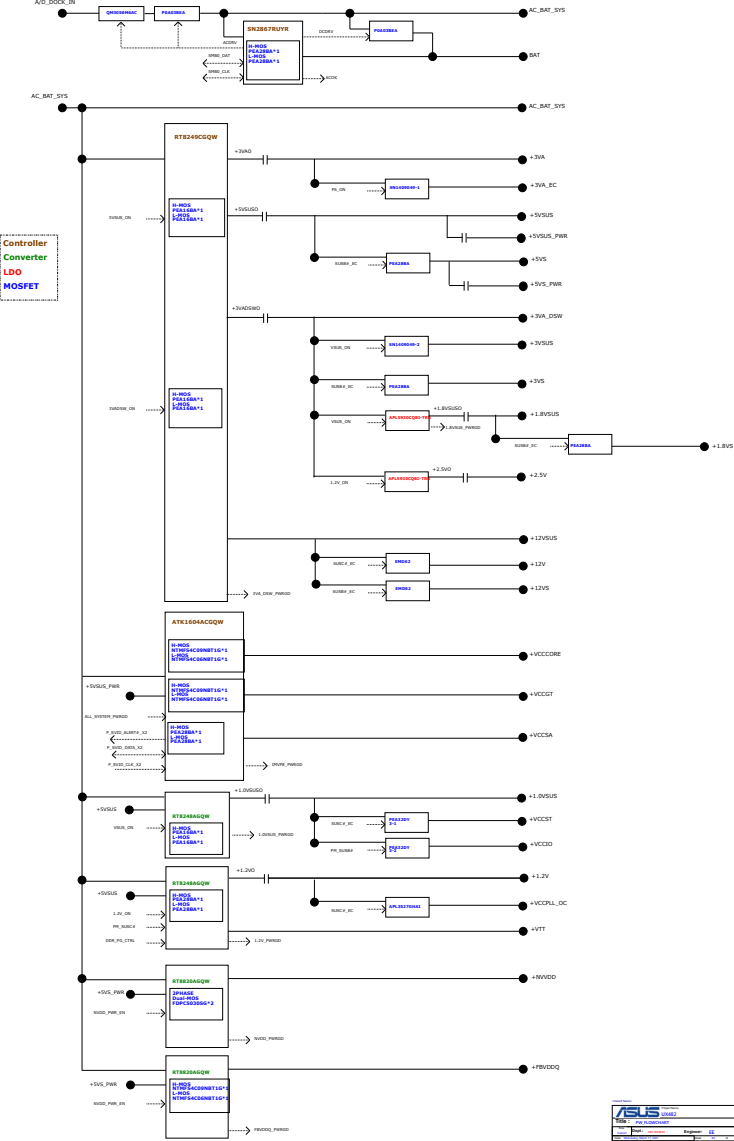


	PU9801	PR9805	PR9807	PC9803	PC9804	PC9805	PR9814	PR9855	PR9822
GN20	NCP454950M7WG 06129-00220000	0 Ohm 10G212000004030	0 Ohm 10G212000004030	⌀	⌀	⌀	0 Ohm 10G212000004030	0 Ohm 10G212000004030	0 Ohm 10G212000004030
N18P-G1	UP90260QK1 06129-00110100	75KOhm 10G212750214010	75KOhm 10G212750214010	1000PF/50V 11G232110214321	1000PF/50V 11G232110214321	0.015UF/16V 11G232115311360	357Ohm 10G212357014010	⌀	49.9Ohm 10G21249R914010

	PC9810	PR9860	PR9809	PR9810	PR9834	PR9863	PR9859	PC9809	PR9808
GN20	⌀	⌀	⌀	10KOhm 10G212100214010	31.6KOhm 10G212316214010	0 Ohm 10G212000004030	0 Ohm 10G212000004030	⌀	⌀
N18P-G1	1000PF/16V 11G232110211030	0 Ohm 10G212000004030	360KOhm 10G212364004010	680KOhm 10G212680314010	324KOhm 10G212324314010	⌀	⌀	0.015UF/16V 11G232115311360	487Ohm 10G212487014010

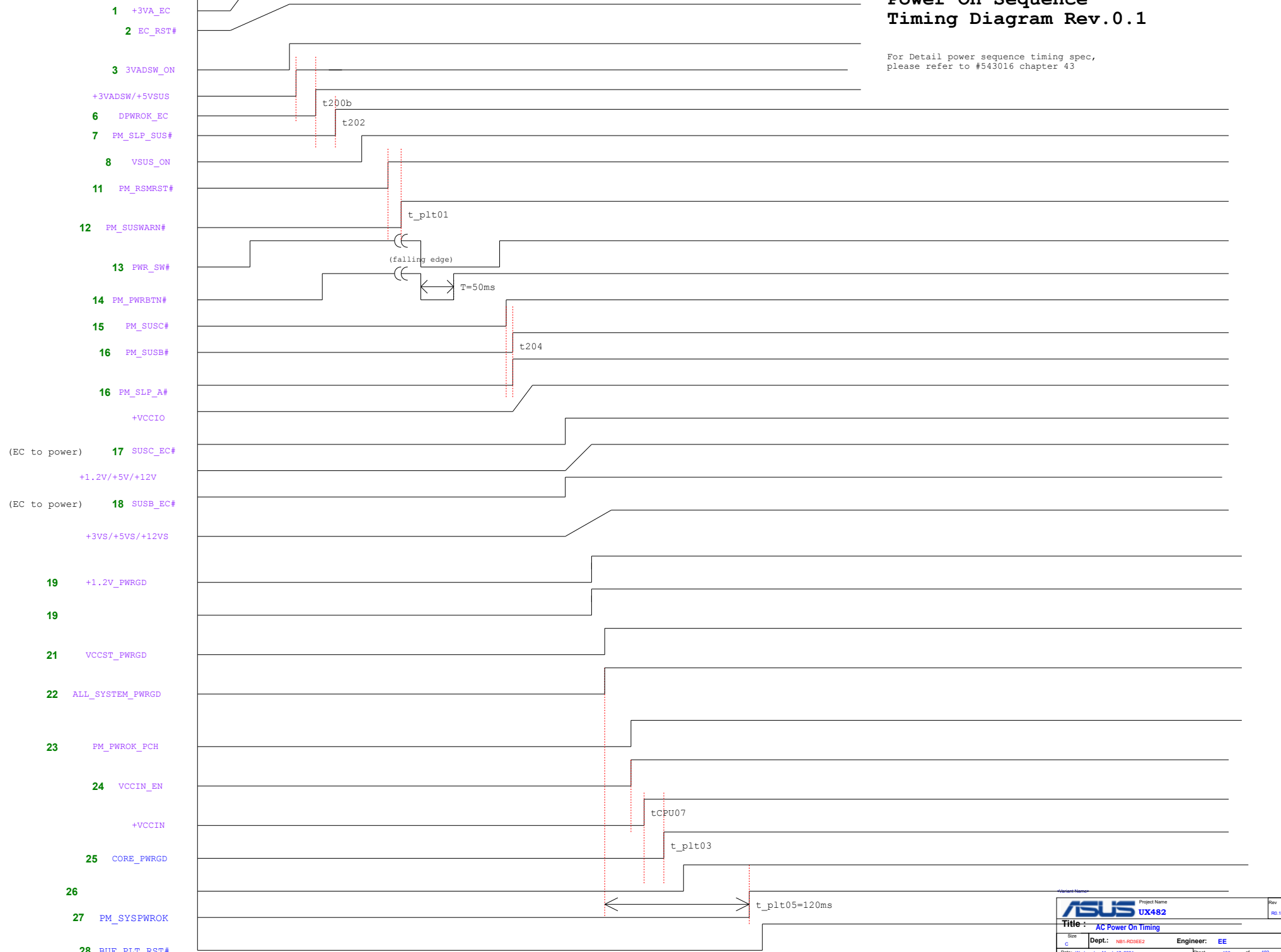
	PR9806	PR9861	PR9864	PR9857	PR9801	PR9853	PR9817	PR9844/PR9845	PR9846/PR9847
GN20	⌀	0 Ohm 10G212000004030	⌀	10KOhm 10G212100214010	0 Ohm 10G212000004030	0 Ohm 10G212000004030	⌀	0 Ohm 10G212000004030	⌀
N18P-G1	487Ohm 10G212487014010	⌀	0Ohm 10G212000004030	⌀	100Ohm 10G212100014010	49.9Ohm 10G21249R914010	357Ohm 10G212357014010	⌀	0 Ohm 10G212000004030

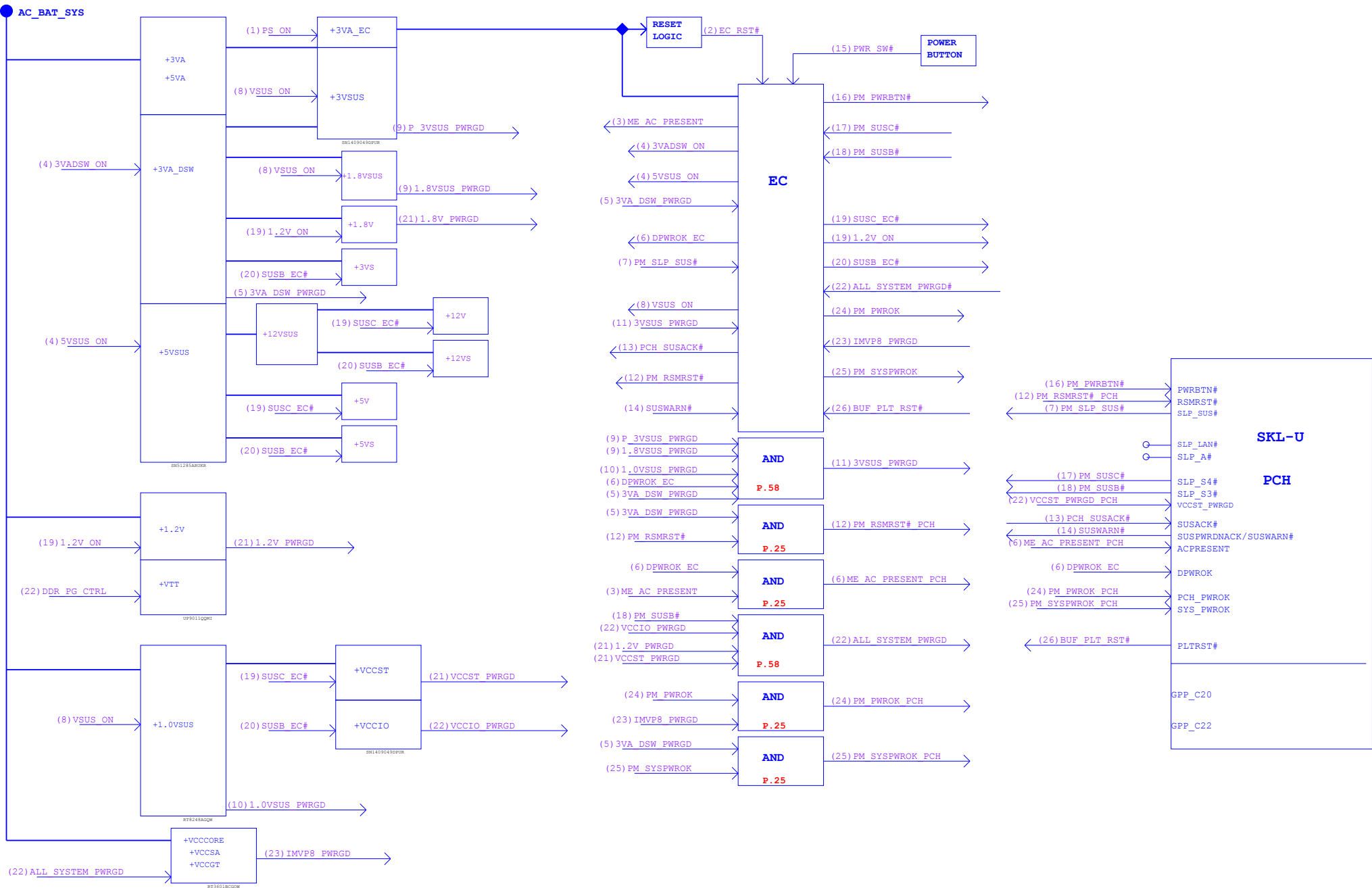
©2021 ASUS



Power-On Sequence Timing Diagram Rev.0.1

For Detail power sequence timing spec,
please refer to #543016 chapter 43





SODIMM CHB-DIMM0
TOP H4.0mm STD (J1601)

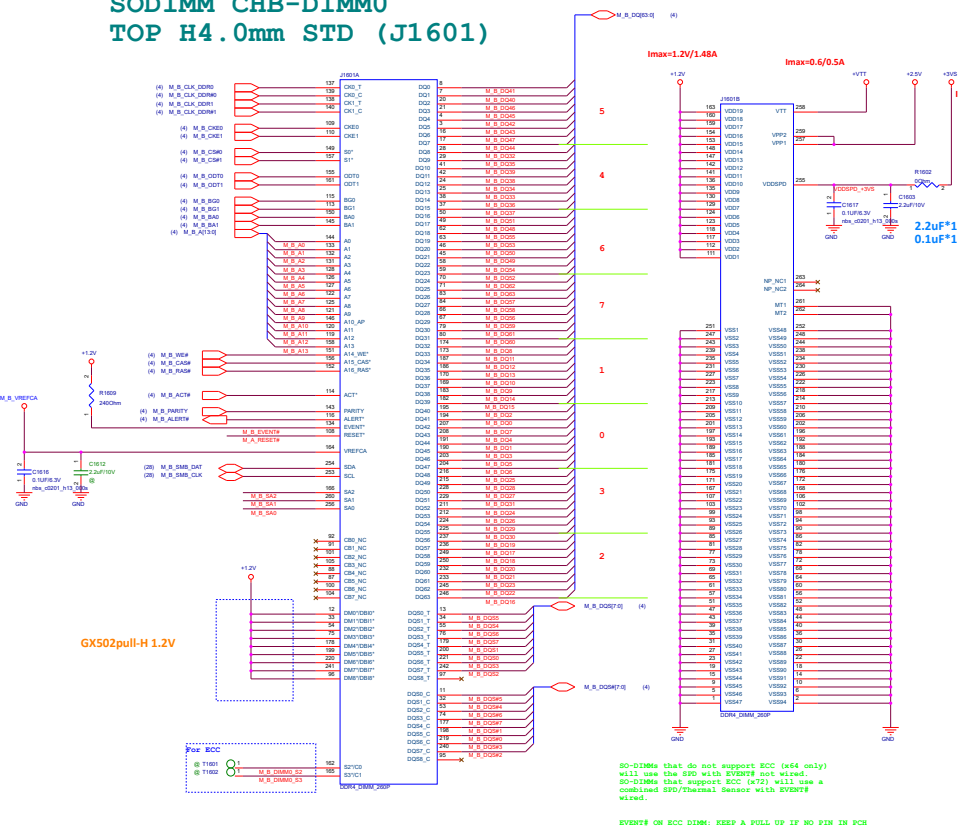
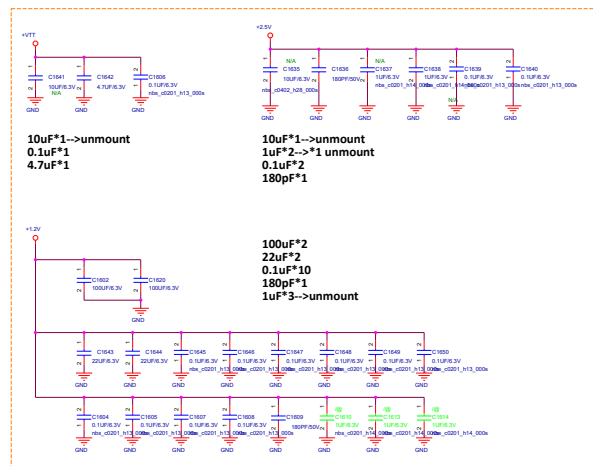
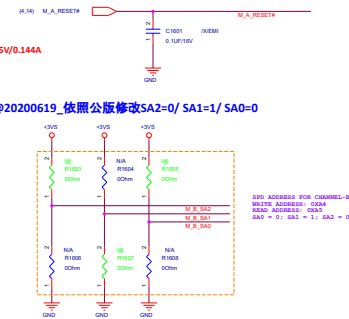


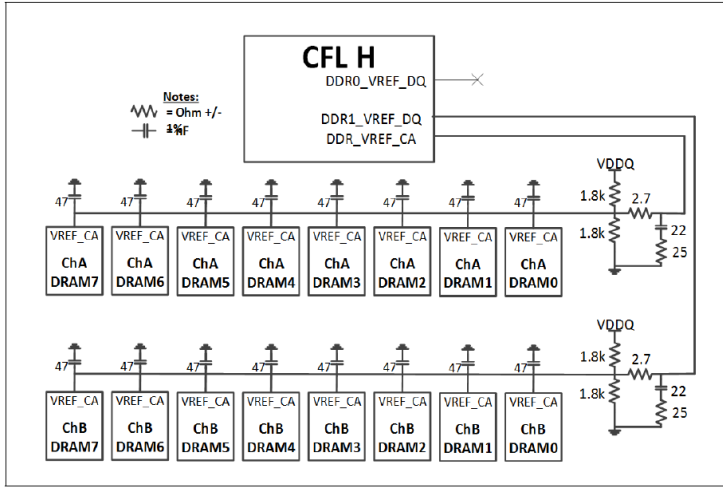
Table 4-24. DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x μ F (size)
DDR4 2 Channels SODIMM 1DPC	VDDQ	4 near each side of the DIMM connector close to VDD pins	16x 10 μ F (0603)
		4 near each side of the DIMM connector close to VDD pins	16x 1 μ F (0402)
		1 placeholder	1x 330 μ F (7343)
	VTT	Placed on VTT plane close to DIMM, 1 cap stuffed, 1 placeholder	2x 10 μ F (0603)
		Placed on VTT plane close to DIMM	4x 1 μ F (0402)
	VPP	DIMM Pin side, 1 per DIMM	2x 10 μ F (0603)
		DIMM Pin side, 1 per DIMM	2x 1 μ F (0402)
	VDDSPD	Place close to DIMM	2x 0.1 μ F (0402)
		Place close to DIMM	2x 2.2 μ F (0402)



Follow FP6 CRB CAP number
@20190701A

Figure 4-24. CFL-H DDR4 x8 Memory Down V_{REF-CA} Overview



Memory Down Vref

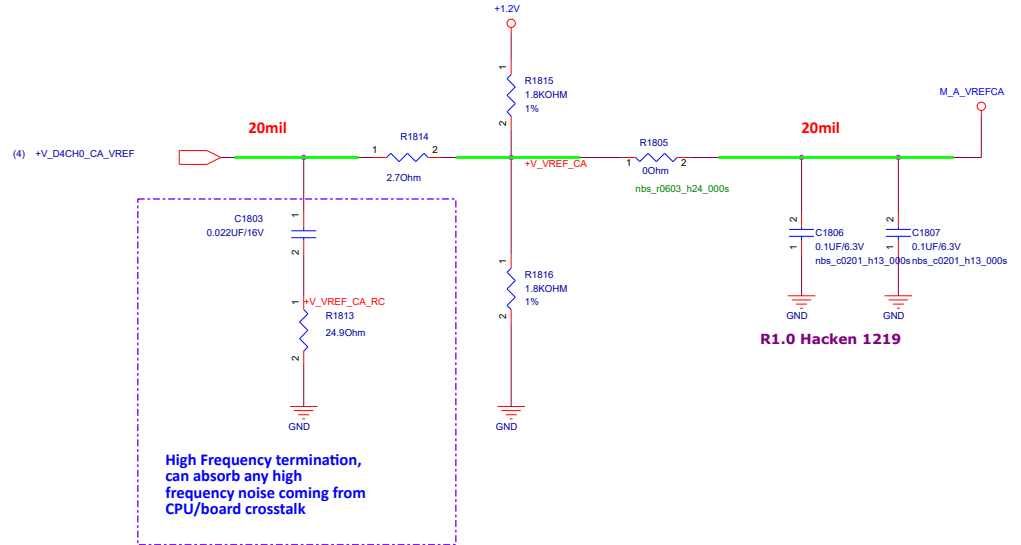
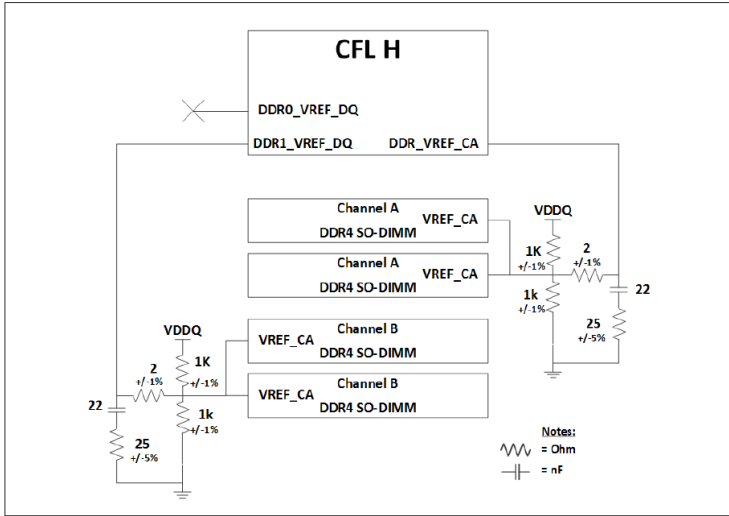
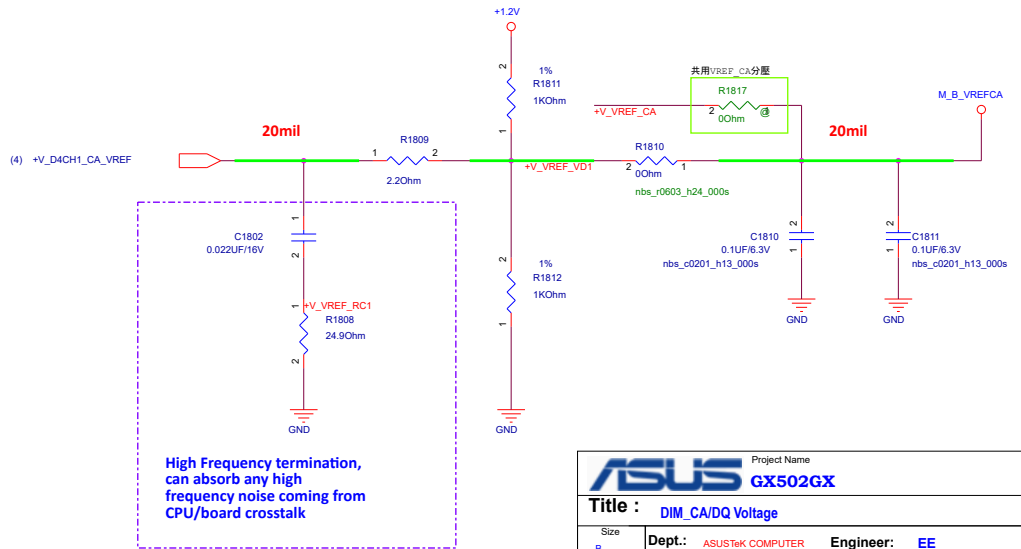


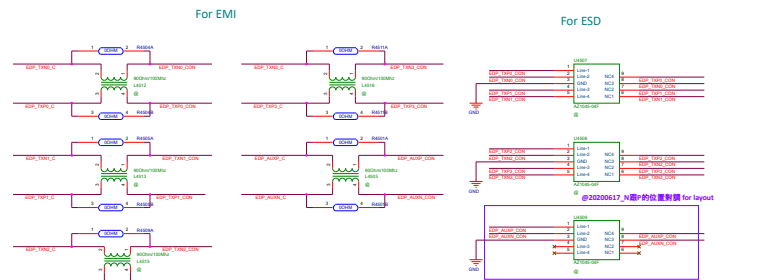
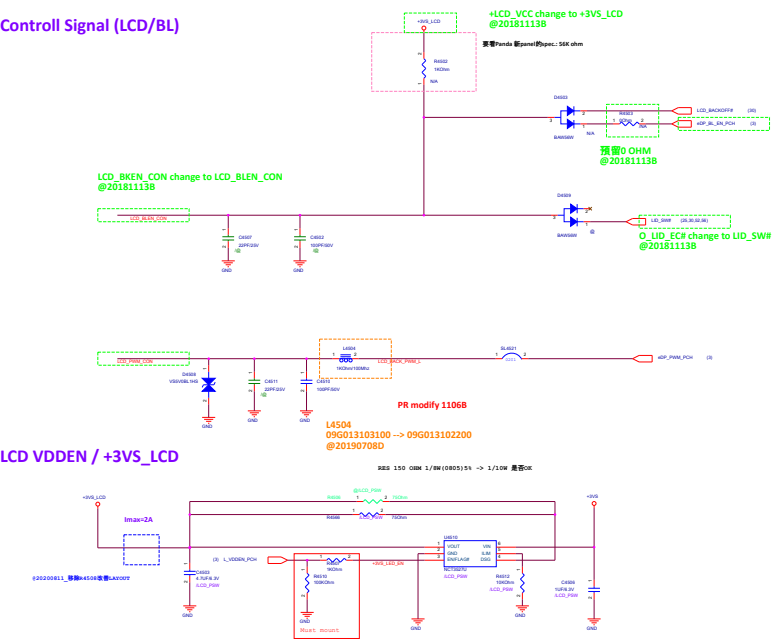
Figure 4-22. CFL-H DDR4 SO-DIMM V_{REF-CA} Overview



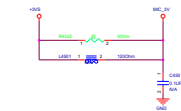
SO-DIMM1 Vref



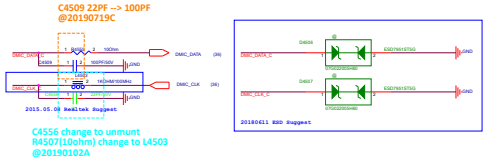
LCD VDDEN / +3VS_LCD



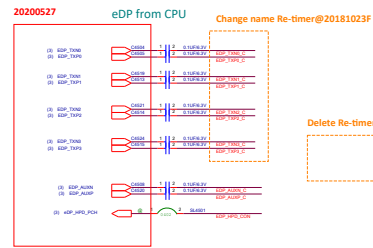
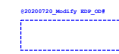
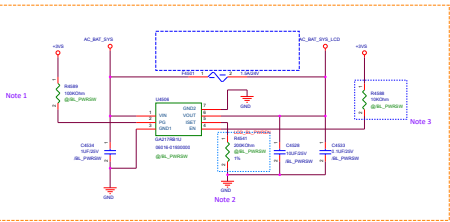
MIC module



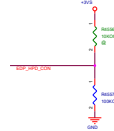
MIC



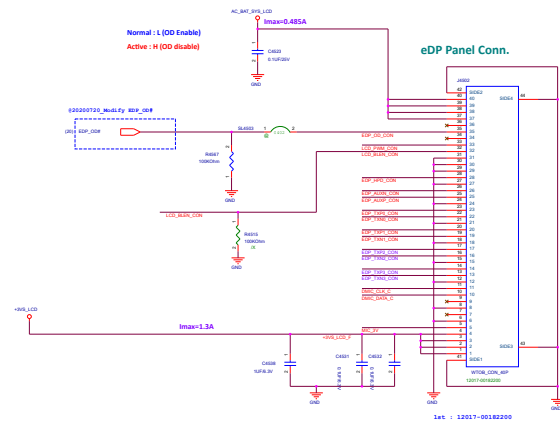
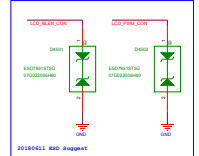
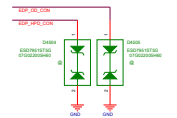
Panel BL Power



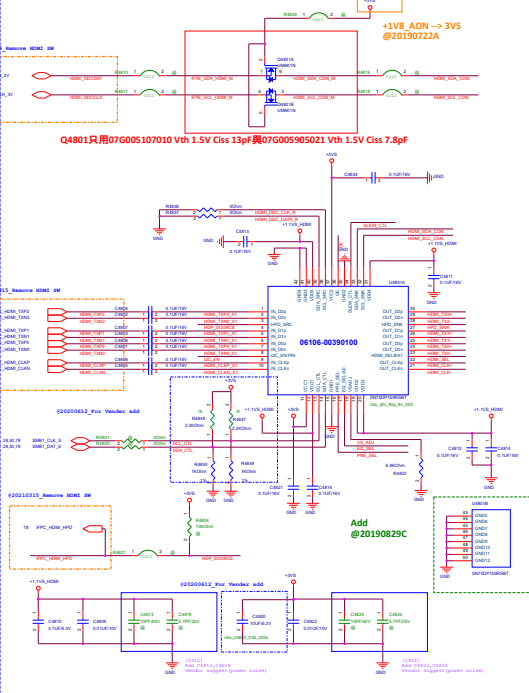
eDP_HPD (CPU)



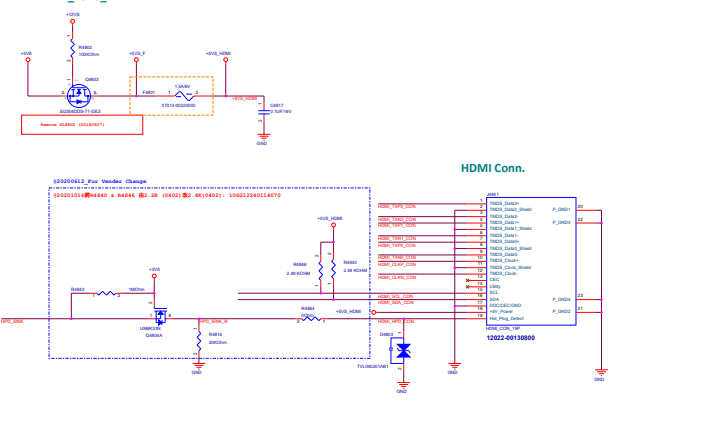
For ESD



Main Board



HDMI Conn.



Add Co-lay device
@20190626E

HDMI Switch

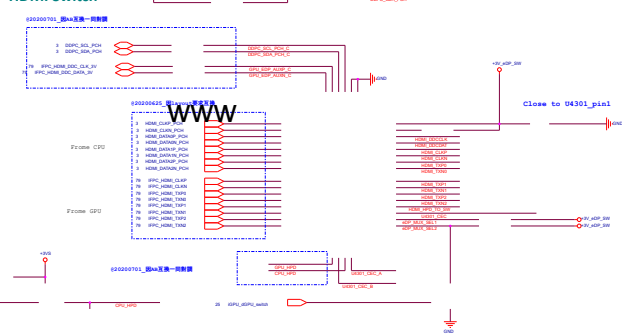
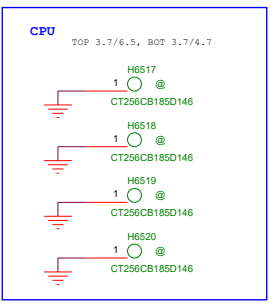
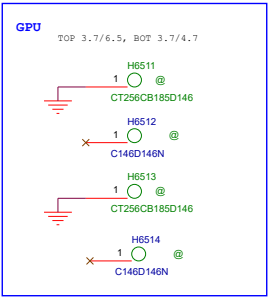
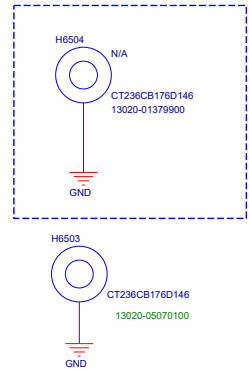
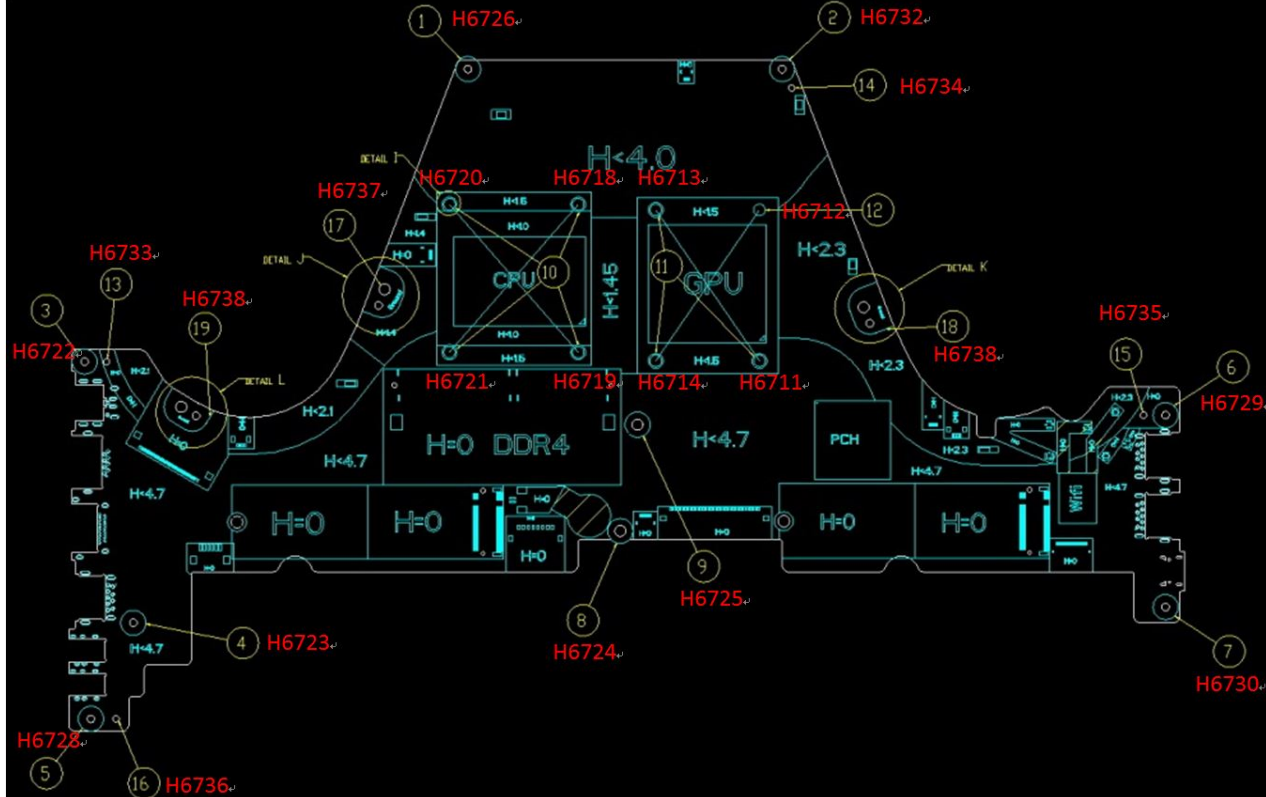


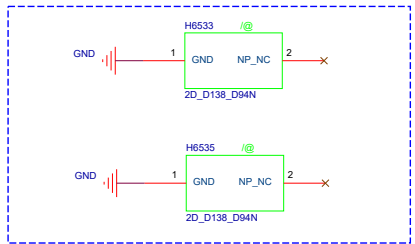
Diagram illustrating the process of RNA polymerase II (RNAP II) transcribing DNA. The top part shows the RNAP II complex (orange) moving along a DNA template (black line), synthesizing an RNA strand (red line) in the 5' to 3' direction. The bottom part shows the RNAP II complex (orange) moving along a DNA template (black line), synthesizing an RNA strand (red line) in the 5' to 3' direction. The diagram is labeled with "RNAP II" and "RNA".

IN	SEL1	SEL2	FUNCTION
L	N	N	Switch Disabled. All Channel Hi-Z.
N	N	L	Channel 1 Enabled. Channel 2 Hi-Z. (Default)
N	N	N	Channel 1 Hi-Z. Channel 2 Enabled.

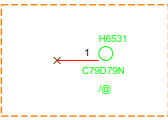
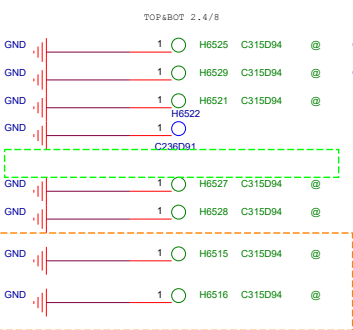
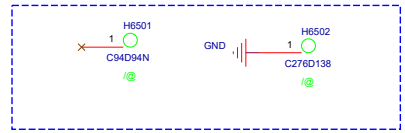
<code>GCPU - GCPU_maxtasks</code>	0	1 (Default)
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@20200707_Modify H6533&H6535

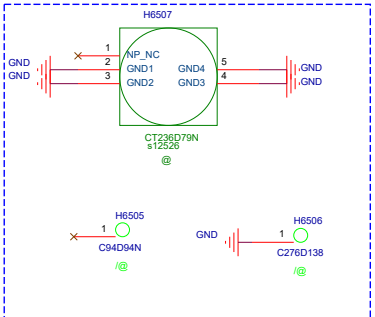
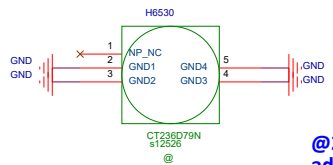
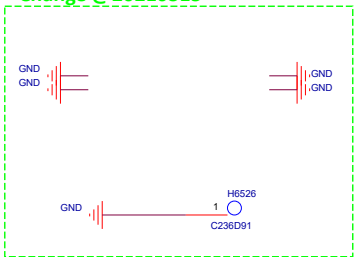


@20200629_del H6534 change H6501 & H6502



Change @20181023F
NC @20181030B

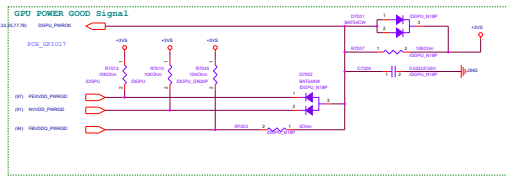
Change @20210315



@20200706_del H6532 change H6506 & H6505 add H6507

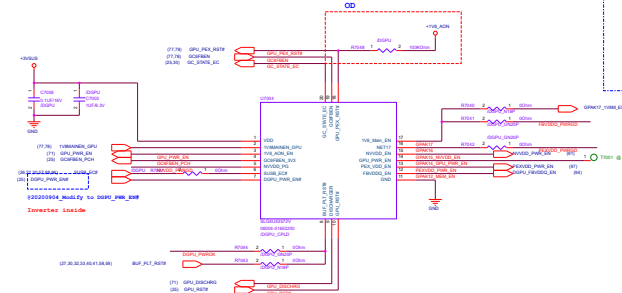


Add @20181029C

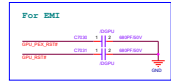


CPID add optional for GM20 and N18P
20200816 ashton modify

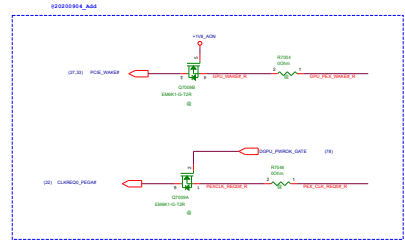
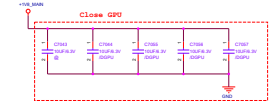
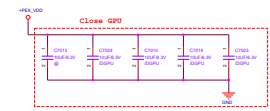
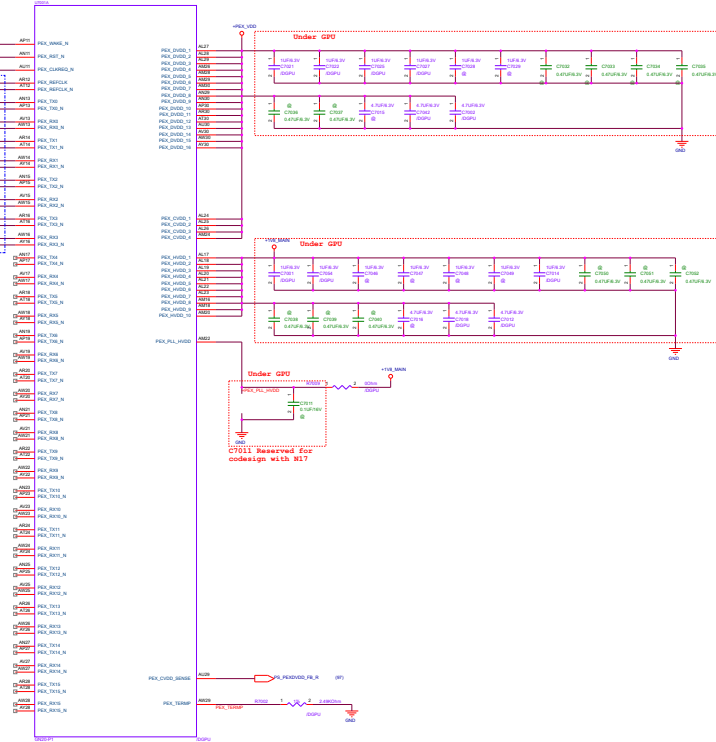
GPU POWER SEQUENCE CONTROL

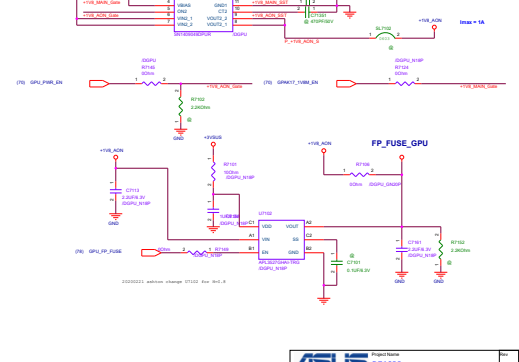
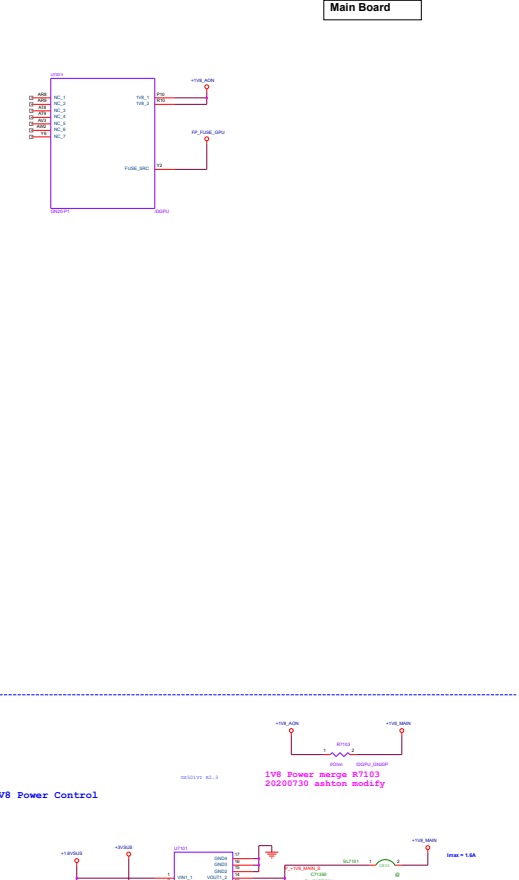


Cydonal	Part Reference	N18P Part number	GM20 Part number	Remark
DGPU_GN20P	R7045, R7041, R7042, R7044, R7103, R7106, R7808, R7809, R7814			GN20P系列需要上件
DGPU_N18P	D7040, D7041, D7043, D7047, C7026, R7040, R7043, R7102, C7113, C7161, C7159, R7101, R7149, R7154, R7802, R7813, R7864, R7815			GN18P-G61-A需要上件
DGPU_CFLD	U7004	00004-01490100	00004-01550300	N18P與GN20P 使用CFLD對應料號
DGPU_ROM	U7802	05006-00041600	05006-00072600	N18P與GN20P 使用ROM對應料號
DGPU_VREF	R7205	100212496914010	100212249114030	N18P與GN20P VREF分壓上down電阻不同
DGPU_VGA				SV301算UMA SKU, for APU only use
VRAM				FOR GPU VRAM 的VIO BOM

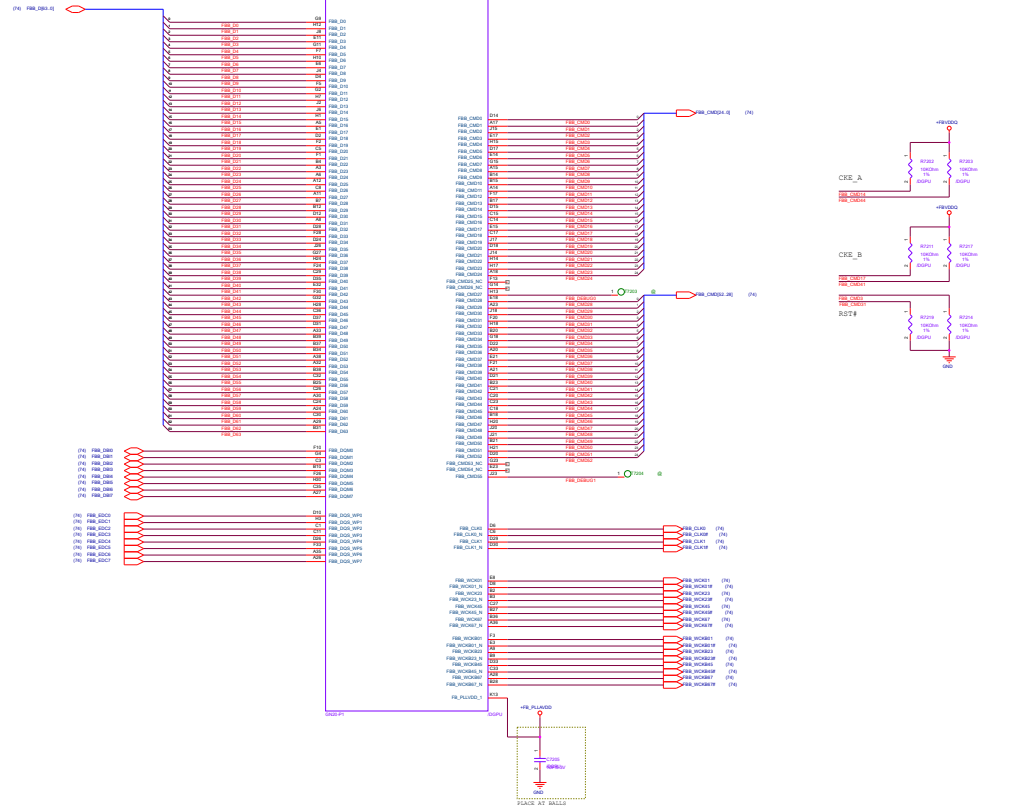


PCI EXPRESS_Graphics REVERSED Type PCIe X16





MEMORY: GPU FB Partition B



FB Pin	What to do for GBS-128	What to do for GBSB-128
FB_YREF	Pull down to 49.9 ohm + 3.9 pF Refer to <i>N1SP-G61-A GeForce GPU Platform Development Package (PDP-01900-001)</i>	Pull down to 2.49 kΩ + 3.9 pF

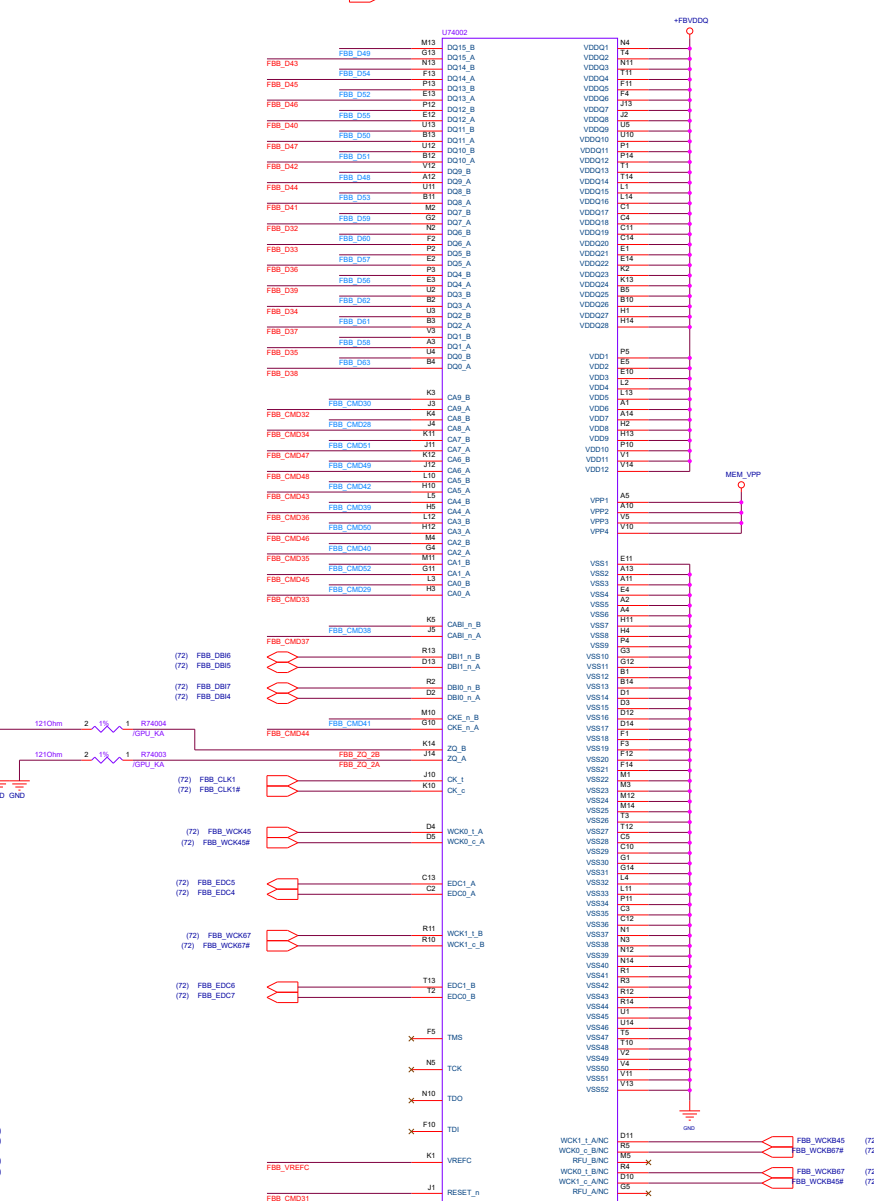
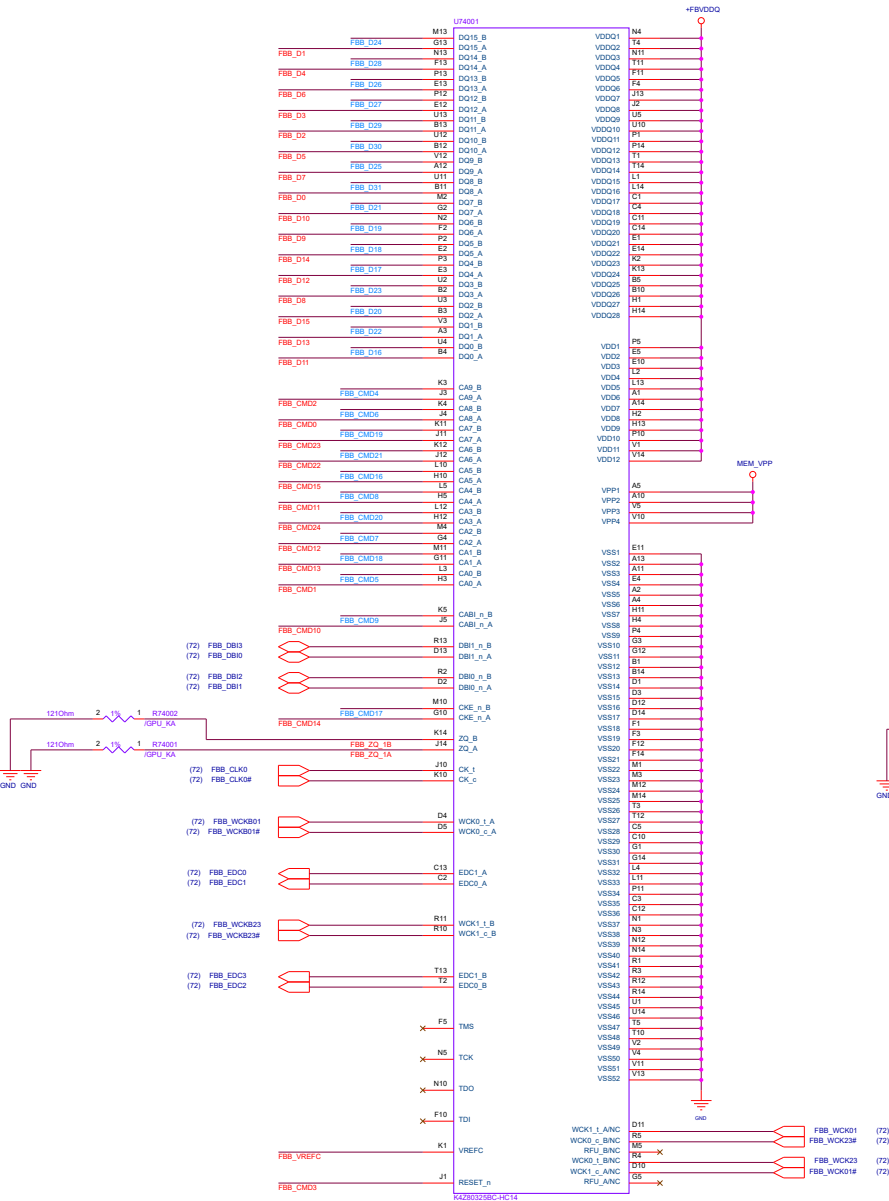
FB Pin	What to do for GBS-128	What to do for GBSB-128
FB_YREF	Pull down to 49.9 ohm + 3.9 pF Refer to <i>N1SP-G61-A GeForce GPU Platform Development Package (PDP-01900-001)</i>	Pull down to 2.49 kΩ + 3.9 pF

40 OHM NET

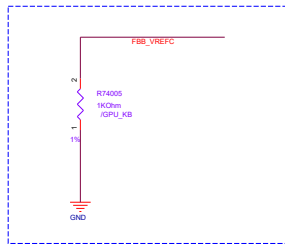
FBB Partition 31..0

40 OHM NET

FBB Partition 64..32

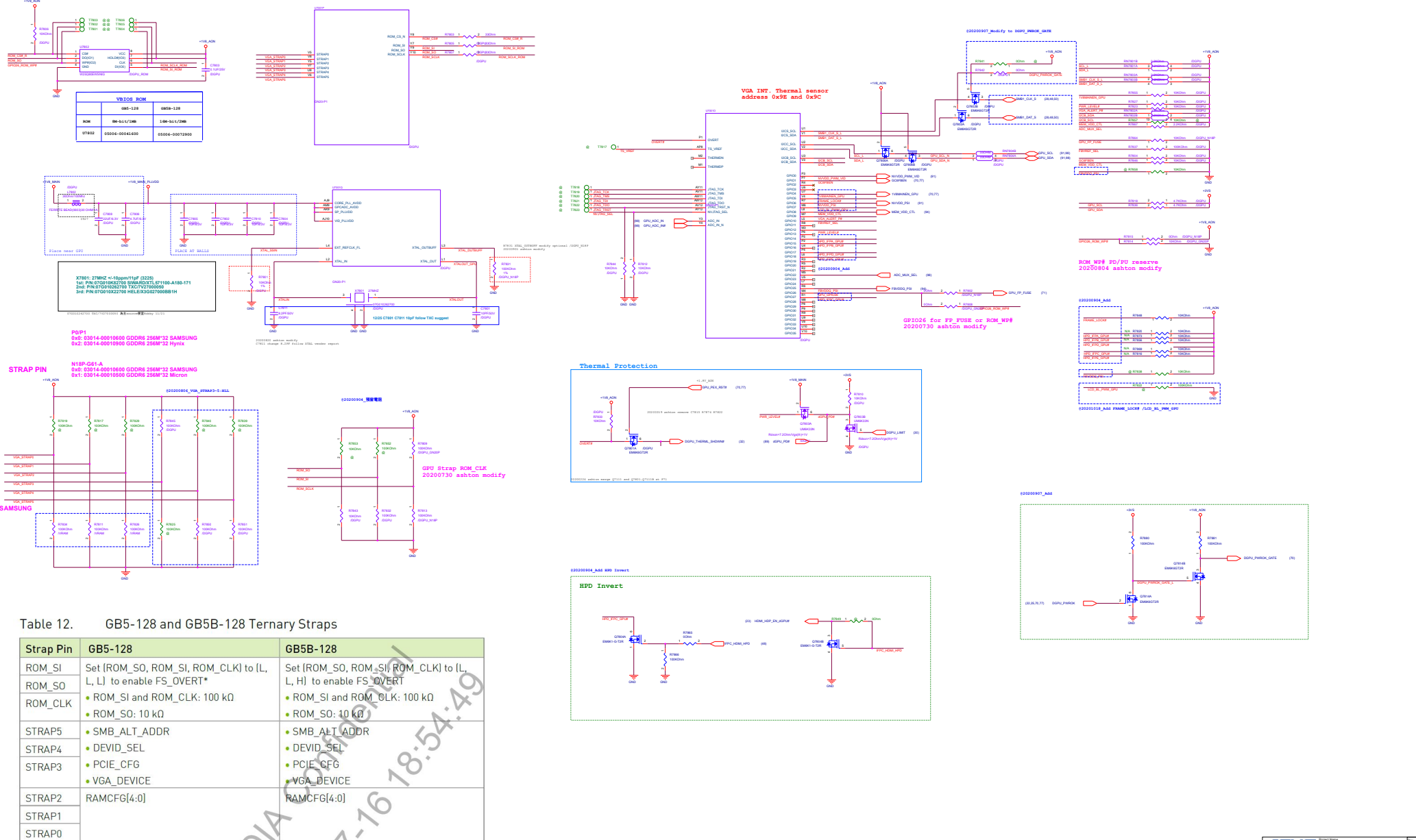


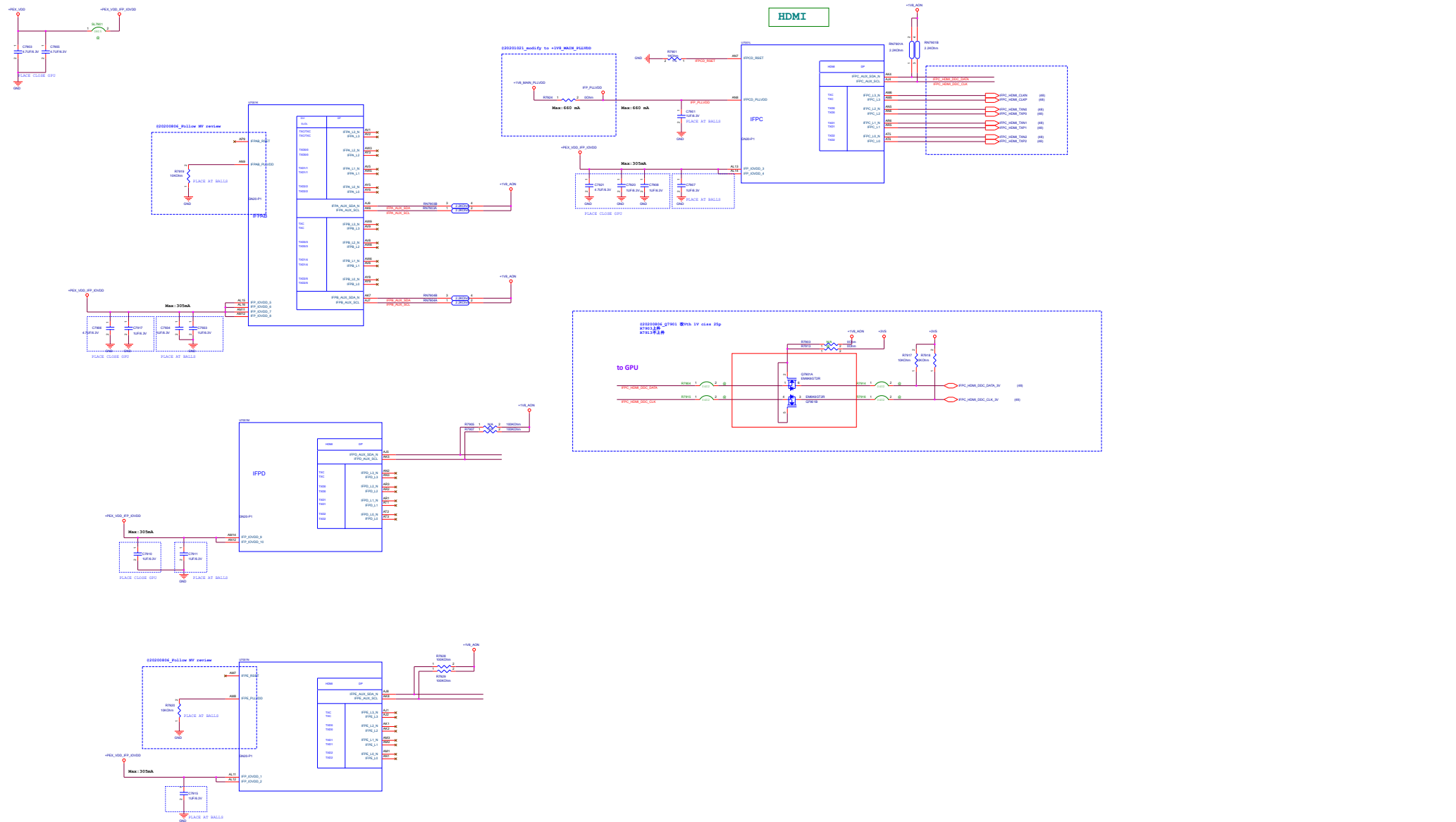
Integrated VREF reference



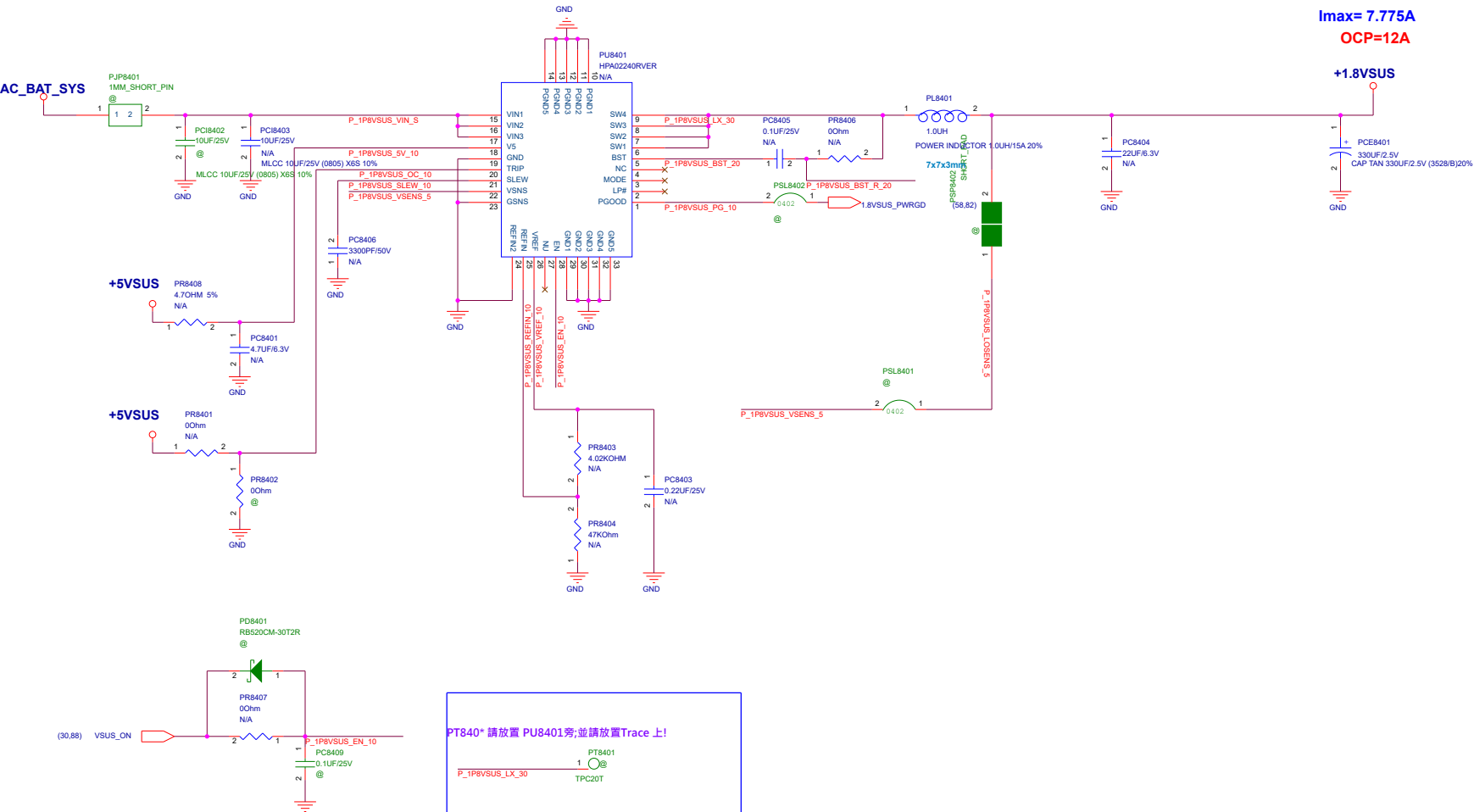
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File	<Title>
Size	Document Number
C	G512L1
Date	Wednesday, March 17, 2021
Sheet	14 of 102
Rev	R1.0





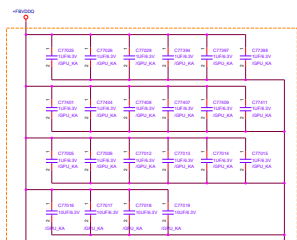
+1.8VSUS [For PCH]



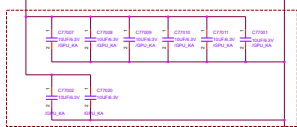
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ASUS		Project Name	Rev
Project Name			R1.0
Title : PW_+1.8VSUS			
Size	Dept.:	Engineer:	Power RD
A3	NB Power team		
Date: Wednesday, March 17, 2021	Sheet	84	of 102

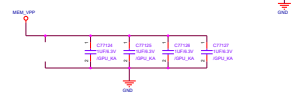
Under DRAM
1uF x 18pcs
10uF x 4pcs



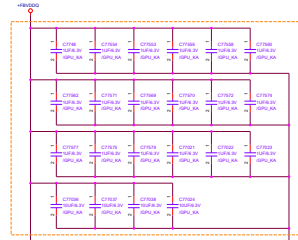
Around DRAM
22uF x 6pcs
10uF x 2pcs



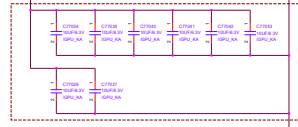
Under DRAM
1uF x 4pcs
4.7uF x 1pcs



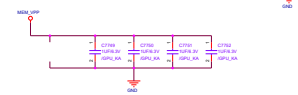
Under DRAM
1uF x 18pcs
10uF x 4pcs



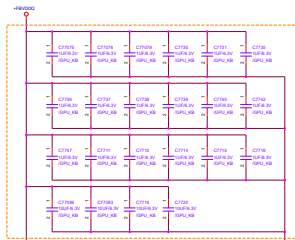
Around DRAM
22uF x 6pcs
10uF x 2pcs



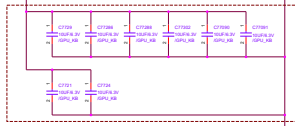
Under DRAM
1uF x 4pcs
4.7uF x 1pcs



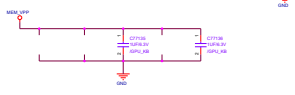
Under DRAM
1uF x 18pcs
10uF x 4pcs



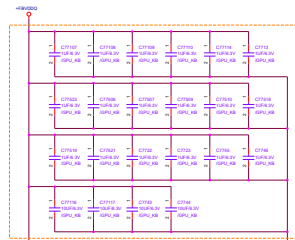
Around DRAM
22uF x 6pcs
10uF x 2pcs



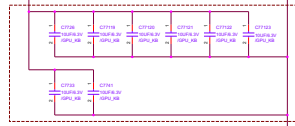
Under DRAM
1uF x 4pcs
4.7uF x 1pcs



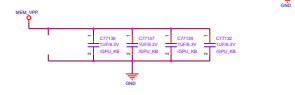
Under DRAM
1uF x 18pcs
10uF x 4pcs



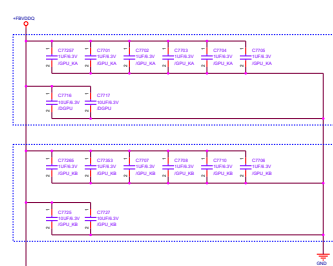
Around DRAM
22uF x 6pcs
10uF x 2pcs



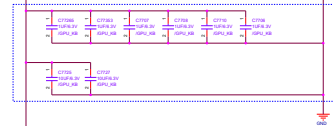
Under DRAM
1uF x 4pcs
4.7uF x 1pcs



Partition A
Under GPU
1uF x 6pcs
10uF x 2pcs



Partition B
Under GPU
1uF x 6pcs
10uF x 2pcs



Close GPU
10uF x 2pcs
22uF x 5pcs

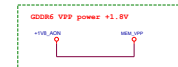


FBVDDQ (GPU side) ¹	1.35V 1.5V	24 x 0.47uF (0201W X65) 4 x 10uF (0603 X65)	2 x 10uF (0603 X65) ² 5 x 22uF (0603 X65)
Alternate solution: 12 x 1uF (0402 or 0201W, X65) ³ 4 x 10uF (0603 X65)			

Table 8.12 DRAM-Side Decoupling

Decoupling Capacitors		Recommended Quantity and Placement (per DRAM device)	
Capacitance	Type, [Size] ^{NOTE 1}	Quantity	Placement
VDD/VDDQ Rail			
0.47 uF ^{NOTE 2}	X65 [0201W]	36	Under or very close to DRAM
10 uF	X65 [0603]	4	Around DRAM
10 uF	X65 [0603]	2	
22 uF	X65 [0603]	6	
VPP Rail			
0.47 uF ^{NOTE 3}	X65 [0201W]	4	Under or very close to DRAM
4.7 uF	X65 [0603]	1	

For power sequence measurement



0201W 0.47uF (0201W X65) 1.35V 1.5V